

SEARCH REQUEST FORM

Scientific and Technical Information Center

121

Requester's Full Name: STEPHEN ELMORE Examiner #: 71664 Date: 2-26-04
 Art Unit: 2186 Phone Number 30 8-6256 Serial Number: 09/749,750
 Mail Box and Bldg/Room Location: CCK2-2C19 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: "LOW POWER CACHE ARCHITECTURE"

Inventors (please provide full names): SUBRAMANIAM MAITHEAN & LYMAN MOULTON

Earliest Priority Filing Date: 12-28-2000

For Sequence Searches Only Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.

CLAIMED INVENTION IS DRAWN TO BOTH A POWER CONTROL METHOD IN AN INTEGRATED CIRCUIT WHICH FUNCTIONS BY DISABLING PORTIONS OF A CACHE (I.E., WAYS, FIELDS, TAG, OR A VICTIM ALLOCATION UNIT) IN RESPONSE TO A MICROINSTRUCTION BY MEANS OF A SINGLE STEP OF A METHOD, OR, DRAWN TO A CACHE CONTROL METHOD BASED ON DISABLING VARIOUS PORTIONS OF A CACHE (SEE ABOVE) IN RESPONSE TO AN ~~INSTR~~ INSTRUCTION OR MICROINSTRUCTION.

CLAIMS 7-19 ARE VERY BROAD AND, IF ALLOWED, MAY BE GIVEN NATIONAL PROMINENCE OR BE SUBJECT TO CRITICISM FOR BEING TOO BROAD.

SYNONYMS ARE: BANKS <=> WAYS <=> CACHE LINES
MODULES <=> BLOCKS

SEE ATTACHED ABSTRACT + CLAIMS

STAFF USE ONLY

	Type of Search	Vendors and cost where applicable
Searcher: <u>Geoffrey St. Leger</u>	NA Sequence (#) _____	STN _____
Searcher Phone #: <u>308-7800</u>	AA Sequence (#) _____	Dialog <u>✓</u>
Searcher Location: <u>4830</u>	Structure (#) _____	Questel/Orbit _____
Date Searcher Picked Up: <u>3/5/4</u>	Bibliographic <u>✓</u>	Dr.Link _____
Date Completed: <u>3/8/4</u>	Litigation _____	Lexis/Nexis _____
Searcher Prep & Review Time: <u>40</u>	Fulltext <u>✓</u>	Sequence Systems _____
Clerical Prep Time: _____	Patent Family _____	WWW/Internet _____
Online Time: <u>230</u>	Other _____	Other (specify) _____



STIC Search Report

EIC 2100

STIC Database Tracking Number: 115414

TO: Stephen Elmore
Location: 2C19
Art Unit : 2186
Monday, March 08, 2004

Case Serial Number: 09/749750

From: Geoffrey St. Leger
Location: EIC 2100
PK2-4B30
Phone: 308-7800

geoffrey.stleger@uspto.gov

Search Notes

Dear Examiner Elmore,

Attached please find the results of your search request for application 09/749750. I searched Dialog's foreign patent files and technical databases.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B30/308-7800

File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)

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File 348:Derwent WPIX 1963-2004/UD,UM &UP=200415

(c) 2004 Thomson Derwent

File 349:EUROPEAN PATENTS 1978-2004/Feb W05

(c) 2004 European Patent Office

File 349:PCT FULLTEXT 1979-2002/UB=20040304,UT=20040226

(c) 2004 WIPO/Univentio

Set	Items	Description
S1	40	AU=(MAIYURAN, S? OR MAIYURAN S? OR MOULTON, L? OR MOULTON - L?)
S2	20	S1 AND CACH???
S3	10	S2 AND POWER(3N) (CONSUM? OR CONSERV?)

3/5/1 (Item 1 from File: 350)
DIALOG(R) File 350:Derwent WPIX.
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014938887 **Image available**

WPI Acc No: 2002-759596/200282

XRFX Acc No: N02-598143

Processor cache for integrated circuit, has clusters of memory cells in each bank, that are associated with half of total number of ways in cache

Patent Assignee: MAIYURAN S J (MAIY-I); MOULTON L (MOUL-I)

Inventor: MAIYURAN S J ; MOULTON L

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020129201	A1	20020912	US 2000749750	A	20001228	200282 B

Priority Applications (No Type Date): US 2000749750 A 20001228

Patent Details:

Patent No	Kind	Lang	Pg	Main IPC	Filing Notes
US 20020129201	A1		14	G06F-013/00	

Abstract (Basic): US 20020129201 A1

NOVELTY - The cache (100) has cache entries (110) that are organized into sets and ways. Clusters of memory cells in each bank of the cache are associated with a half of the total number of ways in the cache.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Power control method; and

(2) Cache control method.

USE - Processor cache for integrated circuits.

ADVANTAGE - Reduces power consumption significantly.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the processor cache.

Cache (100)

Cache entries (110)

pp; 14 DwgNo 1/6

Title Terms: PROCESSOR; CACHE ; INTEGRATE; CIRCUIT; CLUSTER; MEMORY; CELL; BANK; ASSOCIATE; HALF; TOTAL; NUMBER; WAY; CACHE

Derwent Class: T01; U14

International Patent Class (Main): G06F-013/00

File Segment: EPI

File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)

(c) 2004 JPO & JAPIO

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200415

(c) 2004 Thomson Derwent

Set	Items	Description
S1	18772	CACHE? ? OR CACHING
S2	325964	(POWER??? OR SHUT????) (3W)DOWN OR POWERDOWN OR SHUTDOWN OR SHUTTINGDOWN OR DISABL??? OR DEACTIVAT? OR DE()ACTIVAT? OR IN-ACTIV??? OR (TURN??? OR SWITCH??? OR FLIP???? OR TOGGL???) (3W-)OFF OR INOPERAT? OR DISENGAG?
S3	4040111	INDIVIDUAL? OR INDEPENDENT? OR SEPARATE OR SEPARATELY OR P-ARTICULAR OR SELECTED OR SELECT OR SELECTIV? OR SPECIFIC OR C-ERTAIN
S4	4248	S2(7N)S3(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VIC-TIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SUBCOMPONENT? ? OR CONSTITUENT? ?)
S5	4464081	POWER??? OR POWERUP OR ENABL??? OR ACTIVAT? OR (TURN??? OR SWITCH??? OR FLIP???? OR TOGGL???) (3W)ON OR ENGAG??? OR ELECT-RICITY OR CURRENT
S6	59118	S3(7N)S5(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VIC-TIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SUBCOMPONENT? ? OR CONSTITUENT? ?)
S7	15	S1 AND S4
S8	123	S1 AND S6
S9	2411894	POWERUP OR ENABL??? OR ACTIVAT? OR (TURN??? OR SWITCH??? OR FLIP???? OR TOGGL???) (3W)ON OR ENGAG???
S10	28814	S3(7N)S9(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VIC-TIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SUBCOMPONENT? ? OR CONSTITUENT? ?)
S11	85	S1 AND S10
S12	229001	(POWER OR ELECTRICITY) (3N) (CONSUMPTION OR CONSUMED OR CONS-UME OR CONSUMES OR CONSUMING OR USE OR USED OR USAGE OR EXPEN-DITURE? ? OR SAV??? OR CONSERV? OR UTILIZ? OR UTILIS? OR PRES-ERV? OR SPENT OR SPENDING)
S13	25	S8 AND S12
S14	125	S1(15N)S2(15N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR V-ICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SEGMENT? ? OR CONSTITUENT? ?)
S15	15	S12 AND S14
S16	14	S15 NOT (S7 OR S13)

7/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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03673814 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, SEMICONDUCTOR STORAGE DEVICE AND
CONTROL CIRCUIT THEREFOR

PUB. NO.: 09-288614 [JP 9288614 A]
PUBLISHED: November 04, 1997 (19971104)
INVENTOR(s): YAMAZAKI AKIRA
DOSAKA KATSUMI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-100146 [JP 96100146]
FILED: April 22, 1996 (19960422)
INTL CLASS: [6] G06F-012/08; G06F-012/06
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors,
MOS); R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)

ABSTRACT

PROBLEM TO BE SOLVED: To raise the **cache** hit rate of a processor with a
built-in DRAM (dynamic random access memory) and to make power consumption
small.

SOLUTION: The DRAM is provided with **banks** (1-1-1-N) each of whose
activity/ inactivity are mutually **independently** driven. Since the
activity/ inactivity of each of the **banks** (1-1-1-N) are controlled by
respectively mutually **independently** operated row controllers (6-1-6-N), a
page (word line) is turned to a selection state in the respective banks,
a page hit ratio is raised, the number of times of array precharging
operations at the time of a page error is reduced correspondingly to it and
the power consumption is made small.

7/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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03570749 **Image available**
CACHE MEMORY

PUB. NO.: 03-233649 [JP 3233649 A]
PUBLISHED: October 17, 1991 (19911017)
INVENTOR(s): ITSUKIDA SATOSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 02-031157 [JP 9031157]
FILED: February 08, 1990 (19900208)
INTL CLASS: [5] G06F-012/08; G06F-012/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1299, Vol. 16, No. 17, Pg. 19,
January 16, 1992 (19920116)

ABSTRACT

PURPOSE: To improve efficiency for using a memory for an entire processor
by outputting an output from a **cache** memory part to either a **cache**
output or a register output according to a **cache** enable signal.

CONSTITUTION: When a **cache** memory part 110 is not used as a **cache**, a
signal showing the **cache** is **disabled** is applied from a **cache** enable
signal line 102 to an address select circuit 107, input data select
circuit 109 and **cache** output select circuit 12. As a result, an address
subtracting the set data of a data setting means 104 from a register
address on a register address line 105 by a subtraction circuit 106, and a
register input on a register input line 8 are applied to the **cache** memory

part 110 and the output of the **cache** memory part 110 is sent to a register output line 114. Thus, the **cache** memory part 110 can be used as added regist and the memory in the processor can be effectively used.

7/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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03248541 **Image available**
CACHE MEMORY CONTROL CIRCUIT

PUB. NO.: 02-224041 [JP 2224041 A]
PUBLISHED: September 06, 1990 (19900906)
INVENTOR(s): MAEMURA KOJI
APPLICANT(s): NEC IC MICROCOMPUT SYST LTD [470861] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-291396 [JP 88291396]
FILED: November 17, 1988 (19881117)
INTL CLASS: [5] G06F-012/08; G06F-012/08
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1134, Vol. 14, No. 530, Pg. 59, November 21, 1990 (19901121)

ABSTRACT

PURPOSE: To execute the operation at a high speed without increasing the circuit scale by providing a write buffer circuit which can select whether data to the write buffer is inputted from a **cache** memory or inputted from a write data register, by separating it by a byte unit.
CONSTITUTION: In the case when data width of write to a **cache** memory 1 is under one word, a read/write control circuit 7 executes write to a write buffer 102 by making a **cache** data **selective** signal line 71a inactive, making **cache** data **selective** signal lines 71b, 71c and 71d active and making a write data write signal 72 active. As a result, the byte corresponding to 102a and the byte corresponding to 102b, 102c, and 102d are written exclusively in a single cycle from a write data register 3 and the **cache** memory 1, respectively. In such a way, write can be executed in the time being fewer by one cycle than a conventional example.

7/5/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015834703 **Image available**
WPI Acc No: 2003-896907/200382
XRPX Acc No: N03-715812

Vehicle load carrier for transport of goods, has retainer selectively engaging or disengaging locking caches, to lock permit rotation of pivot joint and frame in stowed or deployed position

Patent Assignee: YAKIMA PROD INC (YAKI-N)

Inventor: DEAN G A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030057245	A1	20030327	US 2001298213	P	20010612	200382 B
			US 2002163258	A	20020603	

Priority Applications (No Type Date): US 2001298213 P 20010612; US 2002163258 A 20020603

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030057245	A1	13	B60R-009/00		Provisional application US 2001298213

Abstract (Basic): US 20030057245 A1

NOVELTY - A pivot joint (30) pivotably connects coupling (14) with carrier section (16) of a frame (12). A non-removable retainer (50) selectively engages or disengages locking caches, to lock pivot

joint and frame in either stowed or deployed position or to permit rotation of pivot joint and frame between the two positions.

USE - For transport of recreational and sporting goods like skis, skis, coolers and gears.

ADVANTAGE - The retainer effectively locks pivot joint, such that coupling and carrier section are locked in either deployed or stowed position. The retainer can be easily extended by hand to lock the carrier section with coupling.

DESCRIPTION OF DRAWING(S) - The figure shows the isometric view of the load carrier.

pp; 13 DwgNo 1/9

Title Terms: VEHICLE; LOAD; CARRY; TRANSPORT; GOODS; RETAIN; SELECT; ENGAGE ; DISENGAGE; LOCK; LOCK; PERMIT; ROTATING; PIVOT; JOINT; FRAME; STOW; DEPLOY; POSITION

Derwent Class: Q17

International Patent Class (Main): B60R-009/00

File Segment: EngPI

7/5/5 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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015495623 **Image available**

WPI Acc No: 2003-557770/200352

XRFX Acc No: N03-443391

Cache memory manufacturing yield improving method for computer system, involves disabling defective cache blocks and operating remaining cache blocks without performing cache addressing modification

Patent Assignee: CHERABUDDI R (CHER-I); KASINATHAN M (KASI-I)

Inventor: CHERABUDDI R; KASINATHAN M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030088811	A1	20030508	US 2001839057	A	20010420	200352 B

Priority Applications (No Type Date): US 2001839057 A 20010420

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 20030088811 A1 8 G06F-011/00

Abstract (Basic): US 20030088811 A1

NOVELTY - The defects in cache blocks of a cache memory (13) are determined. The defective cache block is disabled and remaining cache blocks are operated, without performing cache addressing modifications.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for cache memory.

USE - For improving manufacturing yield of multi-way associative cache memory (claimed) in microprocessor cache system of computer system.

ADVANTAGE - Increases manufacturing yield of the cache memory without using expensive redundancy address mapping overhead by selectively disabling defective cache blocks during cache write operation, thereby reducing size and complexity of memory circuit.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the computer system.

cache memory (13)

pp; 8 DwgNo 1/3

Title Terms: CACHE ; MEMORY; MANUFACTURE; YIELD; IMPROVE; METHOD; COMPUTER ; SYSTEM; DISABLE; DEFECT; CACHE ; BLOCK; OPERATE; REMAINING; CACHE ; BLOCK; PERFORMANCE; CACHE ; ADDRESS; MODIFIED

Derwent Class: T01

International Patent Class (Main): G06F-011/00

File Segment: EPI

7/5/6 (Item 3 from file: 350)
DIALOG(R) File 350: Derwent WPIX
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015403729 **Image available**
WPI Acc No: 2003-465869/200344
XRPX Acc No: N03-370551

Memory for data processing system, has power down control circuitry that prevents precharging of the bit lines, while ensuring that memory cells are not selected, in power down mode

Patent Assignee: ARM LTD (ARMA-N)
Inventor: BRAUER M L; PIEJKO A R; SILLA M A; WILLIAMS G R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6552949	B1	20030422	US 200262567	A	20020205	200344 B

Priority Applications (No Type Date): US 200262567 A 20020205

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6552949	B1	19	G11C-007/00	

Abstract (Basic): US 6552949 B1

NOVELTY - A pair of bit lines (515,525) is arranged such that relative change in voltage level between the bit lines indicates the data value stored within the memory cell selected in evaluation phase following precharging phase. A power down control circuitry prevents precharging of the bit lines and the selector circuitry ensures that the memory cells are not selected, in a power down mode.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method for operating memory.

USE - Memory e.g. cache memory for data processing system.

ADVANTAGE - Reduces leakage current in power down mode of operation, by preventing precharging of bit lines during power down mode.

DESCRIPTION OF DRAWING(S) - The figure shows a circuit diagram of the memory.

precharge transistors (505)

bit lines (515,525)

pp; 19 DwgNo 4A/4

Title Terms: MEMORY; DATA; PROCESS; SYSTEM; POWER; DOWN; CONTROL; CIRCUIT; PREVENT; PRECHARGED; BIT; LINE; ENSURE; MEMORY; CELL; SELECT; POWER; DOWN; MODE

Derwent Class: U14; U24

International Patent Class (Main): G11C-007/00

File Segment: EPI

7/5/7 (Item 4 from file: 350)
DIALOG(R) File 350: Derwent WPIX
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015251624 **Image available**
WPI Acc No: 2003-312550/200330
XRPX Acc No: N03-248958

Server cluster operation method for network services, involves deactivating selected server responsive to decrease in server cluster traffic, so that active servers access portion of memory

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: KISTLER M D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030037268	A1	20030220	US 2001931290	A	20010816	200330 B

Priority Applications (No Type Date): US 2001931290 A 20010816

Patent Details:

Abstract (Basic): US 20030037268 A1

NOVELTY - The accessing of selected server's memory by active servers (110) on server cluster (101) is prevented, when the selected server is powered up. The selected server is deactivated responsive to decrease in server cluster traffic, for permitting the active servers to access portion of memory. A file is retrieved from selected server's file **cache** in response to request received by active servers.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

- (1) server; and
- (2) data processing network.

USE - For operating server cluster connected to client such as desktop or laptop computer, personal digital assistant, network computer or workstation, Internet-enabled phone through gateway connected to wide area network, for network computing and network services.

ADVANTAGE - Reduces power consumption, since the **cache** files in powered-down servers are accessible by active servers, thereby improving performance.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the data processing network.

server cluster (101)
active servers (110)
pp; 10 DwgNo 1/6

Title Terms: SERVE; CLUSTER; OPERATE; METHOD; NETWORK; SERVICE; DEACTIVATE;
SELECT; SERVE; RESPOND; DECREASE; SERVE; CLUSTER; TRAFFIC; SO; ACTIVE;
SERVE; ACCESS; PORTION; MEMORY

Derwent Class: T01; W01

International Patent Class (Main): G06F-001/26

International Patent Class (Additional): G06F-001/28; G06F-001/30

File Segment: EPI

7/5/8 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014284316 **Image available**

WPI Acc No: 2002-105017/200214

Related WPI Acc No: 1999-443732; 2002-048925

XRFX Acc No: N02-078058

Microprocessor for executing multithreaded program in computer, fetches new thread based on stored address in response to **cache** miss indication signal

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: PARADY B

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6295600	B1	20010925	US 96675627	A	19960701	200214 B
			US 99340328	A	19990628	

Priority Applications (No Type Date): US 96675627 A 19960701; US 99340328 A 19990628

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
6295600	B1	11	G06F-015/16	Cont of application US 96675627
				Cont of patent US 5933627

Abstract (Basic): US 6295600 B1

NOVELTY - A thread switching logic (112) receives a thread indicator of load instruction from one execution unit (41) in response to the reception of the **cache** miss indication signal (114). A program address register corresponding to thread indicator is selected to invoke the fetching of a new thread. Dispatch of decoded instruction

from respective selected instruction buffer to execution unit, is disabled and enabled subsequently.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer system.

USE - For use in computer to execute multithreaded program.

ADVANTAGE - The switching between the threads of a program is enabled in response to a long latency event such as load/store operations which triggers a thread switch if there is a miss in specific cache level.

DESCRIPTION OF DRAWING(S) - The figure shows the portion of microprocessor with multithreading capability.

Execution unit (41)

Thread switching logic (112)

Cache miss indication signal (114)

pp; 11 DwgNo 3/7

Title Terms: MICROPROCESSOR; EXECUTE; PROGRAM; COMPUTER; NEW; THREAD; BASED ; STORAGE; ADDRESS; RESPOND; CACHE ; MISS; INDICATE; SIGNAL

Derwent Class: T01

International Patent Class (Main): G06F-015/16

File Segment: EPI

7/5/9 (Item 6 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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Image available**

Pat No: 1997-457103/199742

Pub No: N97-380759

Automatic re-configuration system for multiple-way cache system - has cache fill logic device that selects which one of N sets of tag and data RAMs will be utilised to fill in data retrieved from main memory after cache miss operation

Patent Assignee: UNISYS CORP (BURS)

Inventor: WHITTAKER B E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5666513	A	19970909	US 96583327	A	19960105	199742 B

Priority Applications (No Type Date): US 96583327 A 19960105

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 5666513 A 12 G06F-012/08

Abstract (Basic): US 5666513 A

The system includes N sets of tag rams for holding tag addresses of cache data words residing in each one of N associated sets of data rams each one of the addresses involving an upper byte and a lower byte. N sets of parity rams each the set holds a parity bit for each upper byte address and each lower byte address plus a status parity bit which indicates the parity of the combination of a valid bit (V) and a resource bit (R). Each one of the N sets of tag rams is selectively place on-line or off-line. A switch unit receives enable/disable signals from the maintenance subsystem device for determining which set of the N sets of tag rams will be on-line or off-line. A cache control device checks the upper parity bit, the lower parity bit and the status parity bit. A cache fill logic device selects which one of the N sets of tag and data rams will be utilised to fill in data retrieved from main memory after a cache miss operation.

ADVANTAGE - Enables operator control and maintenance subsystem control of cache -set configurations.

Dwg.3/6

Title Terms: AUTOMATIC; CONFIGURATION; SYSTEM; MULTIPLE; WAY; CACHE ; SYSTEM; CACHE ; FILL; LOGIC; DEVICE; SELECT; ONE; N; SET; TAG; DATA; RAM ; UTILISE; FILL; DATA; RETRIEVAL; MAIN; MEMORY; AFTER; CACHE ; MISS; OPERATE

Derwent Class: T01

International Patent Class (Main): G06F-012/08
International Patent Class (Additional): G06F-013/00
File Segment: EPI

7/5/10 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010268659 **Image available**
WPI Acc No: 1995-169914/199522
XRPX Acc No: N95-133230

Reconfigurable cache memory - selectively inhibits access to damaged segments of cache memory by taking failing area of memory off-line for access by CPU by maintaining on-line access for cache consistency operations

Patent Assignee: AMDAHL CORP (AMDA)
Inventor: HILTON R N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5410668	A	19950425	US 92949583	A	19920923	199522 B

Priority Applications (No Type Date): US 92949583 A 19920923

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5410668	A		13 G06F-013/14	

Abstract (Basic): US 5410668 A

The **cache** memory system includes a buffer having a number of segments storing lines of data in addressable storage locations. A first access path is used for accessing the number of segments in parallel for access by the CPU, and a second access path is provided for access to the number of segments in the buffer in parallel for **cache** consistency access.

Access to damaged segments is **selectively disabled** by inhibiting **tag** match and **line** replacement through the first access path without affecting the second access path. Thus, by **disabling** the first access path to **selected** segments, a damaged segment is reconfigured off- **line** without a quiescent state or an extended clocks off period affecting CPU performance.

USE/ADVANTAGE - Reconfiguration of **cache** memory by removing failing segments of **cache** off-line in response to detection of hard errors in failing segment.

Dwg.2/5b

Title Terms: **CACHE** ; MEMORY; SELECT; INHIBIT; ACCESS; DAMAGE; SEGMENT;
CACHE ; MEMORY; FAIL; AREA; MEMORY; LINE; ACCESS; CPU; MAINTAIN; LINE;
ACCESS; **CACHE** ; CONSISTENCY; OPERATE

Derwent Class: T01

International Patent Class (Main): G06F-013/14
File Segment: EPI

7/5/11 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009812840 **Image available**
WPI Acc No: 1994-092695/199411
XRPX Acc No: N94-072636

Programmable cache memory associating sections of main memory with enable-disable status bit - has selectively addressable storage locations for each memory section, from which data is successively requested, with data reading-storing by cache being inhibited w.r.t. disable bit status

Patent Assignee: ZENITH DATA SYSTEMS CORP (ZENI)
Inventor: OLSON A M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
	A	19940322	US 89435320	A	19891113	199411 B
			US 9317972	A	19930212	

Priority Applications (No Type Date): US 89435320 A 19891113; US 9317972 A 19930212

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5297270	A	12	G06F-013/00	Cont of application US 89435320

Abstract (Basic): US 5297270 A

The system includes a main memory having a number of sections, each including a number of selectively addressable storage locations, a **cache** memory, and an accessing arrangement for successively requesting data from respective locations in the main memory. A control appts. assigns each section of the main memory a changeable status condition which is one of a **caching** enabled status and a **caching** disabled status.

The status condition inhibits reading and storing of data by the **cache** memory when data requested by the accessing **unit** is in one of the **sections** of the main memory having the **caching disabled** status. Alternatively, the controller **selectively** operates the system in a mode in which data in the **cache** memory is updated even when reading of data from the **cache** memory is inhibited.

ADVANTAGE - Operable with memory areas of varying size. Flexible in defining memory addresses for which operation of **cache** memory is not permitted. Minimal additional hardware or software.

Dwg.1/5

Title Terms: PROGRAM; **CACHE** ; MEMORY; ASSOCIATE; SECTION; MAIN; MEMORY; ENABLE; DISABLE; STATUS; BIT; SELECT; ADDRESS; STORAGE; LOCATE; MEMORY; SECTION; DATA; SUCCESSION; REQUEST; DATA; READ; STORAGE; **CACHE** ; INHIBIT ; DISABLE; BIT; STATUS

Derwent Class: T01

International Patent Class (Main): G06F-013/00

File Segment: EPI

7/5/12 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009514070 **Image available**

WPI Acc No: 1993-207606/199326

XRPX Acc No: N93-159694

Data processing system with reconfigurable multi-way associative **cache** memory - has addressable main memory storing data at low speed with associated **cache** memory storing data at high speed with tag

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: COYLE W E; NUECHTERLEIN D W; O'DONNELL K E; SARTORIUS T A; SCHULTZ K D; WOLTERS E M; O'DONNELL K E

Number of Countries: 004 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 549508	A1	19930630	EP 92480180	A	19921130	199326 B
US 5367653	A	19941122	US 91813971	A	19911226	199501

Priority Applications (No Type Date): US 91813971 A 19911226

Other Patents: EP 285172; US 5014195

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 549508	A1	E	20 G06F-012/08	

Designated States (Regional): DE FR GB

US 5367653 A 18 G11C-013/00

Abstract (Basic): EP 549508 A

The system comprises an addressable main memory (104) for storing data at relatively low speed with each main address comprising multiple main memory address bits. Addressable associated **cache** memory stores data from main memory of high speed. This is done at **cache** memory

addresses corresponding to predetermined low order main memory address bits and the **cache** memory assigns a tag with the stored data which corresponds to predetermined high order main memory.

A tag responsive **cache** memory reconfiguring unit (120) stores data at reconfigured **cache** memory addresses corresponding to predetermined low order address bits in combination with at least one significant bit of the tag.

ADVANTAGE - Average access time is improved considerably.

Dwg. 7/8

Title Terms: DATA; PROCESS; SYSTEM; MULTI; WAY; ASSOCIATE; **CACHE** ; MEMORY; ADDRESS; MAIN; MEMORY; STORAGE; DATA; LOW; SPEED; ASSOCIATE; **CACHE** ; MEMORY; STORAGE; DATA; HIGH; SPEED; TAG

Derwent Class: T01

International Patent Class (Main): G06F-012/08; G11C-013/00

File Segment: EPI

7/5/13 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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09091396 **Image available**

WPI Acc No: 1992-218819/199227

MRPX Acc No: N92-166158

Test circuit for semiconductor integrated circuit - facilitates precision testing of circuit including for example large capacity memory circuit and logic circuit

Patent Assignee: TOSHIBA KK (TOKE); TOSHIBA MICROELECTRONICS CORP (TOSZ)

Inventor: NOGAMI K; SHIROTORI T

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 492624	A1	19920701	EP 91122220	A	19911224	199227 B
US 5388104	A	19950207	US 91813444	A	19911226	199512
EP 492624	B1	19970219	EP 91122220	A	19911224	199713
DE 69124735	E	19970327	DE 624735	A	19911224	199718
			EP 91122220	A	19911224	
KR 9600346	B1	19960105	KR 9123915	A	19911223	199905

Priority Applications (No Type Date): JP 90418754 A 19901227

Cited Patents: No-SR.Pub; 2.Jnl.Ref; EP 385591

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 492624	A1	E	18	G11C-029/00	
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Designated States (Regional): DE FR GB

US 5388104	A		16	G11C-029/00	
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EP 492624	B1	E	20	G11C-029/00	
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Designated States (Regional): DE FR GB

JP 90418754	E			G11C-029/00	Based on patent EP 492624
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KR 9600346	B1			G11C-029/00	
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Abstract (Basic): EP 492624 A

The test circuit has several writable/readable memory blocks (M4,M5) with different address spaces and an address decoder for selecting addresses of the memory blocks. Multiple memory blocks share part of addresses in test mode of the memory blocks. Writing in a memory **block** (M4) other than the memory **block** (M5) with the largest address space is **disabled** during a period in which address signals for commonly performing address scan of **individual** memory **blocks** exceeds the address width of that memory block.

A logic circuit supplies address signals. The memory blocks are a **cache** memory.

ADVANTAGE - Permits several memory blocks with different address spaces mounted on same chip to be tested at same time. High precision. Avoids putting any burden on generation of test vectors or test circuit for use in BIST method.

Dwg. 4/8

Title Terms: TEST; CIRCUIT; SEMICONDUCTOR; INTEGRATE; CIRCUIT; FACILITATE;
PRECISION; TEST; CIRCUIT; EXAMPLE; CAPACITY; MEMORY; CIRCUIT; LOGIC;
CIRCUIT
Derwent Class: U13; U14
International Patent Class (Main): G11C-029/00
File Segment: EPI

7/5/14 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008630317 **Image available**
WPI Acc No: 1991-134347/199119
XRPX Acc No: N91-103225

Enhanced locked-bus cycle controller for cache memory - maintains
control of bus by inhibiting hold request to controller while processor
lock cycles are not passed to controller

Patent Assignee: COMPAQ COMPUTER CORP (COPQ)
Inventor: TAYLOR M E; CULLEY P R; TAYLOR M
Number of Countries: 008 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 425843	A	19910508	EP 90119257	A	19901008	199119 B
CA 2026816	A	19910504				199128
US 5163143	A	19921110	US 89431742	A	19891103	199248
EP 425843	A3	19920708	EP 90119257	A	19901008	199334

Priority Applications (No Type Date): US 89431742 A 19891103

Cited Patents: NoSR.Pub; EP 400840

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 425843	A			
Designated States (Regional): BE DE FR GB IT NL				
US 5163143	A	10	G06F-012/06	

Abstract (Basic): EP 425843 A

The system provides a **cache** control register or port wherein the value of the specified bits sets the locked bus cycle operation to one of three modes. Mode one passes all processor locked cycles to the **cache** controller simulating the prior Intel method. Mode two disables the locked **cache** controller from operating in a locked mode.

Mode three provides an enhanced locked cycle methodology which allows most locked cycles from the processor to execute out of **cache** memory and allows multiprocessing with shared memory without increasing the possibility of semaphore errors.

ADVANTAGE - Increased operating speed. (11pp Dwg.No.1/3

Title Terms: ENHANCE; LOCK; BUS; CYCLE; CONTROL; **CACHE** ; MEMORY; MAINTAIN;
CONTROL; BUS; INHIBIT; HOLD; REQUEST; CONTROL; PROCESSOR; LOCK; CYCLE;
PASS; CONTROL

Derwent Class: T01

International Patent Class (Main): G06F-012/06

International Patent Class (Additional): G06F-013/36

File Segment: EPI

7/5/15 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004836716
WPI Acc No: 1986-340057/198652
XRPX Acc No: N86-253772

Memory management of microprocessor system - converting virtual to
physical address using segment and page descriptors

Patent Assignee: INTEL CORP (ITLC)
Inventor: CRAWFORD J H; RIES P; RIES P S
Number of Countries: 009 Number of Patents: 012

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3618163	A	19861218	DE 3618163	A	19860530	198652 B
GB 2176918	A	19870107	GB 8519991	A	19850808	198701
GB 2176920	A	19870107	GB 8612679	A	19860523	198701
FR 2583540	A	19861219				198704
CN 8506711	A	19870204				198817
GB 2176918	B	19891101	GB 8512679	A	19850808	198944
GB 2176920	B	19891122				198947
US 4972338	A	19901120	US 88185325	A	19880419	199049
KR 9005897	B	19900813				199142
US 5173872	A	19921222	US 85744389	A	19850613	199302
			US 8773054	A	19870713	
US 5321836	A	19940614	US 85744389	A	19850613	199423
			US 88185325	A	19880419	
			US 90506211	A	19900409	
DE 3618163	C2	19950427	DE 3618163	A	19860530	199521

Patent Applications (No Type Date): US 85744389 A 19850613; US 88185325 A 19880419; US 8773054 A 19870713; US 90506211 A 19900409

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3618163	A		36		
US 5173872	A		15	G11C-015/04	Cont of application US 85744389
US 5321836	A		19	G06F-012/10	Cont of application US 85744389
					Cont of application US 88185325
					Cont of patent US 4972338
DE 3618163	C2		15	G06F-012/08	

Abstract (Basic): DE 3618163 A

The microprocessor system contains a segmenting mechanism to provide conversion of the virtual address into a second linear address, as well as providing testing and control of the data memory segment attributes. The microprocessor chip (10) is coupled to a main read/write memory (13). The microprocessor is a 32 bit type and operates with a physical address of 32 bits that is generated by the management system that converts 48 bit virtual addresses using either a segmenting or paging method.

The address conversion unit (20) has separate modules for the two techniques with one unit having a segment descriptor register and the other a segment descriptor (21) cache memory (22). Attribute data provides protection of the memory contents of the system. (36pp Dwg.No.1/8)

Title Terms: MEMORY; MANAGEMENT; MICROPROCESSOR; SYSTEM; CONVERT; VIRTUAL; PHYSICAL; ADDRESS; SEGMENT; PACE; DESCRIBE

Derwent Class: T01

International Patent Class (Main): G06F-012/10; G11C-015/04

International Patent Class (Additional): G06F-007/00; G06F-009/34; G06F-012/08

File Segment: EPI

13/5/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014884704 **Image available**

WPI Acc No: 2002-705410/200276

XRPX Acc No: N02-556023

the memory system for superscalar microprocessor, powers and selects memory banks based on state of predetermined bits of received address for data access

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: SHIELL J H; STEISS D E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6442667	B1	20020827	US 9888450	A	19980608	200276 B
			US 99314557	A	19990519	

Priority Applications (No Type Date): US 9888450 P 19980608; US 99314557 A 19990519

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6442667	B1	10	G06F-012/00	Provisional application	US 9888450

Abstract (Basic): US 6442667 B1

NOVELTY - A pair of multiplexers (520-527,535) select cache banks (510-517) powered by decoders (501,505) for data access based on states of specified bits of a received address (31). A buffer (503) provides physical address for specified virtual address bits of received address to select a cache line. A validation unit (530) validates the selected line based on a valid tag indicating a match between cache and received addresses, received from a table (518).

USE - For superscalar microprocessor.

ADVANTAGE - By powering and selecting the cache banks based on the states of predetermined bits of the received address, power consumption of the cache memory is reduced thereby reducing heat generation.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the cache memory system.

Address (31)

Decoders (501,505)

Buffer (503)

Cache banks (510-517)

Table (518)

Multiplexers (520-527,535)

Validation unit (530)

pp; 10 DwgNo 5/5

Title Terms: CACHE ; MEMORY; SYSTEM; MICROPROCESSOR; POWER; SELECT; MEMORY ; BANK; BASED; STATE; PREDETERMINED; BIT; RECEIVE; ADDRESS; DATA; ACCESS

Derwent Class: T01; U14

International Patent Class (Main): G06F-012/00

File Segment: EPI

13/5/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014416786 **Image available**

WPI Acc No: 2002-237489/200229

XRPX Acc No: N02-182758

Cache memory for data processing system, compares tag addresses held in ways with external tag addresses to activate match line connected to that way when both the addresses are identical

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)

Inventor: HOON C; MYUNG K Y; CHOI H; YIM M; LIM M G

Number of Countries: 006 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010026465	A1	20011004	US 2001800685	A	20010307	200229 B
FR 2807176	A1	20011005	FR 20013383	A	20010313	200229
GB 2366046	A	20020227	GB 20016189	A	20010313	200229
JP 2001273193	A	20011005	JP 200136094	A	20010213	200229
KR 2001091109	A	20011023	KR 200012473	A	20000313	200229
US 6317351	B2	20011113	US 2001800685	A	20010307	200229
GB 2366046	B	20021002	GB 20016189	A	20010313	200273
KR 373849	B	20030226	KR 200012473	A	20000313	200345
TW 510990	A	20021121	TW 2001105672	A	20010312	200353

Priority Applications (No Type Date): KR 200012473 A 20000313

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010026465	A1		19	G11C-015/04	
FR 2807176	A1			G06F-012/08	
GB 2366046	A			G06F-012/08	
JP 2001273193	A		13	G06F-012/08	
KR 2001091109	A			G11C-013/00	
US 6317351	B2			G11C-015/04	
GB 2366046	B			G06F-012/08	
KR 373849	B			G11C-013/00	Previous Publ. patent KR 2001091109
TW 510990	A			G06F-012/00	

Abstract (Basic): US 20010026465 A1

NOVELTY - A tag array (560) and a data array (580) has N/M sets with match lines connected to respective K ways. Way selection decoders (540) enabled by a set selection signal, generates way selection signals. The **tag** array compares **tag** addresses in the **selected K ways** with an external **tag** address, to **activate** the match line of that way to a voltage level, when both the addresses are identical.

USE - For microprocessors used in data processing system, embedded system such as hand-held telephone.

ADVANTAGE - The **power consumed** in determining HIT/MISS of the **cache** memory access is decreased. The parallel connection of transistors in the tag array which are connected to the match line improves operating speed.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of **cache** memory.

Way selection decoders (540)

Tag array (560)

Data array (580)

pp; 19 DwgNo 7/10

Title Terms: **CACHE**; MEMORY; DATA; PROCESS; SYSTEM; COMPARE; TAG; ADDRESS; FIELD; WAY; EXTERNAL; TAG; ADDRESS; ACTIVATE; MATCH; LINE; CONNECT; WAY; ADDRESS; IDENTICAL

Derwent Class: T01; U14; W01

International Patent Class (Main): G06F-012/00; G06F-012/08; G11C-013/00; G11C-015/04

International Patent Class (Additional): G11C-011/41; G11C-011/413

File Segment: EPI

13/5/7 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014238755 **Image available**

WPI Acc No: 2002-059453/200208

SRPX Acc No: N02-044062

Cache device for microcomputer, selects and activates specific word lines of objective memory access blocks, based on the offset field in access address

Patent Assignee: SEIKO EPSON CORP (SHIH)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001306395	A	20011102	JP 2000124228	A	20000425	200208 B

Priority Applications (No Type Date): JP 2000124228 A 2000 425

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
JP 2001306395 A 13 G06F-012/08

Abstract (Basic): JP 2001306395 A

NOVELTY - A block of memory cells in a RAM (310) is connected to word lines, selectively. The access objective block is identified based on the index field in access address of CPU. A controller (352) selects and activates specific word lines of access blocks, based on the offset field in the received access address.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

- (a) Semiconductor device;
- (b) Microcomputer;
- (c) Electronic device

USE - For microcomputer (claimed), electronic device (claimed) e.g. notebook PC, portable telephone.

ADVANTAGE - Reduces power consumption by selective activation of memory blocks.

DESCRIPTION OF DRAWING(S) - The figure shows the cache device with word line selector. (Drawing includes non-English language text).

RAM (310)

Controller (352)

pp; 13 DwgNo 4/12

Title Terms: **CACHE** ; DEVICE; MICROCOMPUTER; SELECT; ACTIVATE; SPECIFIC; WORD; LINE; OBJECTIVE; MEMORY; ACCESS; BLOCK; BASED; OFFSET; FIELD; ACCESS; ADDRESS

Derwent Class: T01; U14

International Patent Class (Main): G06F-012/08

International Patent Class (Additional): G06F-015/78; G11C-011/41

File Segment: EPI

pub date:
11/2/01

13/5/8 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013544691 **Image available**

WPI Acc No: 2001-028897/200104

XRPX Acc No: N01-022908

Set associative type cache memory device enables prohibition of usage of specific sets of tags and lines by praxis of exclusive instruction set up by a register

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000298618	A	20001024	JP 99106801	A	19990414	200104 B

Priority Applications (No Type Date): JP 99106801 A 19990414

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
JP 2000298618 A 11 G06F-012/08

Abstract (Basic): JP 2000298618 A

NOVELTY - Several sets of tags and lines are provided collectively. The usage of the specific sets of tags and lines is prohibited by praxis of an exclusive instruction set up by a register (17). An AND gate (16) performs logical AND of read-out control signal supplied to tag and line from a controller (14) with the value stored in register.

USE - Set associative type cache memory device.

ADVANTAGE - Reduces power consumption without reducing hit-rate of cache memory.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic view of the set associative type cache memory device.

Controller (14)

AND Gate (16)

Register (17)
pp; 11 DwgNo 1/10
Title Terms: SET; ASSOCIATE; TYPE; **CACHE** ; MEMORY; DEVICE; ENABLE;
PROHIBIT; SPECIFIC; SET; TAG; LINE; EXCLUDE; INSTRUCTION; SET; UP;
REGISTER
Derwent Class: T01
International Patent Class (Main): G06F-012/08
International Patent Class (Additional): G06F-012/08
File Segment: EPI

13/5/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012979496 **Image available**
WPI Acc No: 2000-151349/200014
XRPX Acc No: N00-112335

Main memory of data processing system - is independent of supply of
power to all units in data processing system

Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000010674	A	20000114	JP 98178497	A	1998062	200014 B

Priority Applications (No Type Date): JP 98178497 A 19980625

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000010674	A	7	G06F-001/26	

Abstract (Basic): JP 2000010674 A

NOVELTY - The display, peripheral and LAN controllers (15, 18,16) and main and **cache** memory units (14,12) are connected to system controller, via PCI bus (17) and memory bus respectively. The power supply system supplies power to each **unit** of the data processing system. The supply of **power** to all **units** in the data processing system is performed **independent** of the **power** supply to non-volatile memory.

USE - For personal computer system.

ADVANTAGE - The hardware of data processing terminal is minimized and thereby reducing space required and cost needed. Enables **saving power** at the time of standby. DESCRIPTION OF DRAWING(S) - The figure shows explanatory hardware block of data processing system. (12,14) Main and **cache** memory units; (15) Display controller; (16) LAN controller; (17) PCI bus; (18) Peripheral controller.

Dwg.1/7

Title Terms: MAIN; MEMORY; DATA; PROCESS; SYSTEM; INDEPENDENT; SUPPLY;
POWER; UNIT; DATA; PROCESS; SYSTEM

Derwent Class: T01
International Patent Class (Main): G06F-001/26
File Segment: EPI

13/5/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012555851 **Image available**
WPI Acc No: 1999-361957/199931
XRPX Acc No: N99-269975

Power supply switching device of single chip microcomputer - includes control unit which releases low power consumption state of internal circuit and performs dynamic low power consumption control when hit information indicates **cache error**

Patent Assignee: HITACHI LTD (HITA); HITACHI MICON SYSTEM KK (HITA-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11134077	A	19990521	JP 97298042	A	19971030	199931 B

Priority Applications (No Type Date): JP 97298042 A 19971030

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11134077	A		14	G06F-001/32	

Abstract (Basic): JP 11134077 A

NOVELTY - A data processor has CPU (2) and **cache** memory (4). When **cache** error is not indicated corresponding to hit information (HIT), the condition of internal circuit is switched to low **power consumption** state. When hit information indicates **cache** error, a **control unit** (41) releases low **power consumption** state of internal circuit and controls dynamic low **power consumption**. DETAILED DESCRIPTION - An **INDEPENDENT CLAIM** is also included for data processing system.

USE - In single chip microcomputer, microprocessor.

ADVANTAGE - Enables appropriate control of **power consumption** condition of module, since there is no need for dynamic operation based on condition of **cache** memory. Reduces **power consumption** of data processor. Reduces wastage of power, since static low **power consumption** opposing peripheral circuit is also used along with dynamic low **power consumption**. Avoids need for **power consumption** in bus controller and input and output circuit, since there is no external access operation. DESCRIPTION OF DRAWING(S) - The figure shows the block diagram indicating the power supply switching device. (2) CPU; (4) **Cache** memory; (41) Control unit.

Dwg.1/10

Title Terms: POWER; SUPPLY; SWITCH; DEVICE; SINGLE; CHIP; MICROCOMPUTER; CONTROL; UNIT; RELEASE; LOW; POWER; CONSUME; STATE; INTERNAL; CIRCUIT; PERFORMANCE; DYNAMIC; LOW; POWER; CONSUME; CONTROL; HIT; INFORMATION; INDICATE; **CACHE**; ERROR

Derwent Class: T01

International Patent Class (Main): G06F-001/32

International Patent Class (Additional): G06F-001/04; G06F-012/08

File Segment: EPI

13/5/11 (Item 9 from file: 350)
 TANDG(R) File 350:Derwent WPIX
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012498847 **Image available**
 WPI Acc No: 1999-304951/199926
 XRPX Acc No: N99-228589

Content addressable memory (CAM)

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: FUNG P K; TRAN H V

Number of Countries: 026 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 920030	A2	19990602	EP 98309665	A	19981125	199926 B
JP 11283378	A	19991015	JP 98334683	A	19981125	200001

Priority Applications (No Type Date): US 9767293 P 19971126

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 920030	A2	E	17	G11C-015/04	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT

LI LT LU LV MC MK NL PT RO SE SI

Patent No	Kind	Date
JP 11283378	A	15 G11C-015/04

Abstract (Basic): EP 920030 A2

NOVELTY - The content addressable memory (CAM) comprises a data **cache** for storing data associated with each tag. A tag memory has rows and columns of tag cells. Each tag cell (10) stores a bit of a tag and has a multiplexing switch (16) to receive a cell output signal

representing the bit-**select** lines each connect cells of one column and **activate** the multiplexing switches of those cells. A number of readlines (15) each connect cells of a row and receive a cell output signal from a cell of that row via the cell's associated multiplexing switch. A tag compare circuit receives cell output signals via each readline and compares a cell output signal on each readline with a signal representing a bit of the target tag. A target tag line sequentially delivers bits of the target tag to the tag compare circuit. A hit line indicates the results of comparisons made by the tag compare circuit. A data bus outputs data from the data **cache** when a tag is matched to the target **tag**. A controller has a control input to receive control signals, and **activate** the bit-**select** lines and generate a readout signal to **activate** the data **cache** such that data associated with a matched **tag** may be retrieved.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of sequentially comparing a target tag to tags stored in a tag memory portion of a content addressable memory.

USE - The CAM is used in a **cache** system. For e.g. packet communications systems.

ADVANTAGE - Reduces die area of memory. Eliminates current spikes by reducing **power consumption**. CAM may be easily programmed to accommodate target tags having varying lengths.

DESCRIPTION OF DRAWING(S) - The drawing shows a tag cell of a CAM.

Tag cell (10)

Readline (15)

Multiplexing switch (16)

pp; 17 DwgNo 2/11

Title Terms: CONTENT; ADDRESS; MEMORY; CAM

Derwent Class: U14

International Patent Class (Main): G11C-015/04

International Patent Class (Additional): G06F-012/08

File Segment: EPI

13/5/12 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012389115 **Image available**

WPI Acc No: 1999-195222/199917

XRPX Acc No: N99-143492

Cache **memory** - outputs indexed data externally by reading data from selected memory cell indicated by access form indication signal to path indicated by path selecting signal

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11039216	A	19990212	JP 97198033	A	19970724	199917 B

Priority Applications (No Type Date): JP 97198033 A 19970724

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11039216	A	9	G06F-012/08	

Abstract (Basic): JP 11039216 A

NOVELTY - The control unit outputs indexed data externally by reading data from selected memory cell indicated by access form indication signal (ATYP) to path indicated by path selecting signal (WSEL). Memory cells are juxtaposed with data array to which two or more paths are assigned.

USE - In secondary semiconductor memory for computer.

ADVANTAGE - Improves through-put of memory. Reduces **power consumption**. Offers burst access such as continuous read access. Enables top priority selection **selectively**.

DESCRIPTION OF DRAWING(S) - The figure shows **block** diagram of semiconductor memory. (ATYP) Access form indication signal; (WSEL) Path selecting signal.

Dwg.1/9

Title Terms: **CACHE** ; **MEMORY**; **OUTPUT**; **INDEX**; **DATA**; **EXTERNAL**; **READ**; **DATA**;
SELECT; **MEMORY**; **CELL**; **INDICATE**; **ACCESS**; **FORM**; **INDICATE**; **SIGNAL**; **PATH**;
INDICATE; **PATH**; **SELECT**; **SIGNAL**
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

13/5/13 (Item 11 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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012347076 **Image available**
WPI Acc No: 1999-153183/199913
Related WPI Acc No: 1996-485348
XRPX Acc No: N99-110456

Instruction fetch system for reduced instruction set computer (RISC)
processor

Patent Assignee: SILICON GRAPHICS INC (SILI-N)
Inventor: KALDANI G G; KOWALCZYK A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5870574	A	19990209	US 9364189	A	19930517	199913 B
			US 95491491	A	19950616	
			US 96686363	A	19960724	

Priority Applications (No Type Date): US 9364189 A 19930517; US 95491491 A
19950616; US 96686363 A 19960724

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5870574	A		9	G06F-009/30	Cont of application US 9364189 Div ex application US 95491491 Div ex patent US 5568442

Abstract (Basic): US 5870574 A

NOVELTY - An instruction selection MUX (84) accesses groups of instructions with different sets of ordered addresses, simultaneously from an instruction **cache** (20). The groups of instructions are executed during specific cycles. The instruction groups are transferred to an instruction decoder (90) during the specified cycles. A program counter (88) generates the sequence of ordered instruction addresses during successive cycles.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the method of fetching instructions in a RISC processor.

USE - RISC processor.

ADVANTAGE - Reduces word **line** lengths thus reducing capacitive loading of word **lines** and **power consumption**. Predecodes **portion** of **cache** addresses on processor to **select particular** segment of **cache** memory. Reduces **power consumption** of memory **modules** and support circuitry by reducing **cache** accesses.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the instruction fetch system.

instruction **cache** (20)
instruction selection (84)
program counter (88)
instruction decoder (90)

pp; 9 DwgNo 5/5

Title Terms: INSTRUCTION; FETCH; SYSTEM; REDUCE; INSTRUCTION; SET; COMPUTER
; PROCESSOR

Derwent Class: T01
International Patent Class (Main): G06F-009/30
International Patent Class (Additional): G06F-012/00
File Segment: EPI

13/5/14 (Item 12 from file: 350)
DIALOG(R) File 350:Derwent WPIX

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011558843 **Image available**

WPI Acc No: 1997-535324/199749

XRPX Acc No: N97-445741

Set associative cache memory - operates in low- power mode by selecting only portions of cache memory needed to perform certain operations

Patent Assignee: BENCHMARK MICROELECTRONICS INC (BENC-N)

Inventor: LAU W; SHEPPARD D P

Number of Countries: 001 Number of Patents: 001

Parent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5682515	A	19971028	US 938207	A	19930125	199749 B
			US 96664319	A	19960610	

Priority Applications (No Type Date): US 938207 A 19930125; US 96664319 A 19960610

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5682515	A		12	G06F-012/00	Cont of application US 938207

Abstract (Basic): US 5682515 A

A four-way **cache** data memory is provided, having a **cache** data RAM (30) and a tag RAM (28). The tag RAM is enabled to access one of the tags. This tag is compared with the tag portion of the received memory address to determine if a tag is stored within. If a true comparison results, a HIT is indicated and this is utilized to enable a portion of the **cache** data RAM.

The data in the enabled portion is then output on the data bus. Additionally, the data output of the **cache** data RAM is inhibited unless it is determined that the **cache** data stored in the **cache** data RAM is valid, this information stored in a status RAM (62).

ADVANTAGE - Has reduced **power** consumption .

Dwg.3/8

Title Terms: SET; ASSOCIATE; **CACHE** ; MEMORY; OPERATE; LOW; POWER; MODE; SELECT; PORTION; **CACHE** ; MEMORY; NEED; PERFORMANCE; OPERATE

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

13/5/15 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011492498 **Image available**

WPI Acc No: 1997-470411/199743

Related WPI Acc No: 1998-520644

XRPX Acc No: N97-392539

Maintaining cache coherency while minimising power consumption - operating 1st MPU at low power consumption , starting 2nd MPU write cycle on system bus to request cache data, snooping write cycle using bus interface of 1st MPU and signalling that modified cache line data is stored in cache of 1st MPU

Patent Assignee: INTEL CORP (ITLC)

Inventor: CARMEAN D M; CRAWFORD J

Number of Countries: 001 Number of Patents: 001

Parent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5669003	A	19970916	US 94363744	A	19941223	199743 B

Priority Applications (No Type Date): US 94363744 A 19941223

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5669003	A		11	G06F-001/32	

Abstract (Basic): US 5669003 A

The method includes operating a first processor in a reduced **power**

mode. While the first processor is operating in a reduced power mode, certain parts of the internal logic in the first processor remain clocked so that the first processor continues to monitor transactions on the system bus. The second processor runs a transaction on the system bus to request data.

In the event that the first processor determines that the transaction by the second processor is requesting cache data that is stored in the first processor in a modified state, the first processor signals the second processor. After the current bus cycle is completed, the first processor writes back the modified cache line on the system bus and second processor re-runs the transaction on the system bus.

ADVANTAGE - Totally transparent interaction with external bus while minimising power consumption.

Dwg.1/5

Title Terms: MAINTAIN; CACHE ; COHERE; MINIMISE; POWER; CONSUME; OPERATE; MPU; LOW; POWER; CONSUME; START; MPU; WRITING; CYCLE; SYSTEM; BUS; REQUEST; CACHE ; DATA; WRITING; CYCLE; BUS; INTERFACE; MPU; SIGNAL; MODIFIED; CACHE ; LINE; DATA; STORAGE; CACHE ; MPU

Derwent Class: T01

International Patent Class (Main): G06F-001/32

File Segment: EPI

13/5/16 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011429570 **Image available**

WPI Acc No: 1997-407477/199738

XRPX Acc No: N97-338899

Solid state memory unit of computer - has switch provided between sense circuit and memory cell arrays of cache memory, which is operated based on part selecting signal to select optimum path

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9179784	A	19970711	JP 95340282	A	19951227	199738 B

Priority Applications (No Type Date): JP 95340282 A 19951227

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9179784	A	12		

Abstract (Basic): JP 9179784 A

The memory unit has a cache memory with several paths. The cache memory has memory cell arrays (CMA1,CMA2) to store a part of the data stored by a main memory. A path selection signal is generated based on the tag information.

A switch (SW) is inserted between the memory cell arrays and a sense circuit (SA). Optimum part is selected by the operation of the switch, based on the path selection signal.

ADVANTAGE - Restrains power consumption even with increase in number of paths.

Dwg.1/11

Title Terms: SOLID; STATE; MEMORY; UNIT; COMPUTER; SWITCH; SENSE; CIRCUIT; MEMORY; CELL; ARRAY; CACHE ; MEMORY; OPERATE; BASED; PART; SELECT; SIGNAL; SELECT; OPTIMUM; PATH

Derwent Class: T01; U14; U21

International Patent Class (Main): G06F-012/08

International Patent Class (Additional): G06F-012/10; G11C-011/41

File Segment: EPI

13/5/17 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011302705 **Image available**

WPI Acc No: 1997-280610/199725

Related WPI Acc No: 1993-128239; 1996-068606; 1996-341870; 1999-034507;
1999-478185

Invalidating cache memory in low-power state - has logic circuit that powers up integrated circuit in reduced power consumption state to run invalidation cycle in cache memory and places integrated circuit back into reduced power consumption state after invalidation cycle has completed

Patent Assignee: INTEL CORP (ITLC)

Inventor: BEUTLER R R; CONARY J W

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5630146	A	19970513	US 91778575	A	19911017	199725 B
			US 9336470	A	19930324	
			US 95543523	A	19951016	

Priority Applications (No Type Date): US 9336470 A 19930324; US 91778575 A 19911017; US 95543523 A 19951016

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5630146	A		26	G06F-001/32	CIP of application US 91778575 Cont of application US 9336470 Cont of patent US 5481731

Abstract (Basic): US 5630146 A

Circuitry places the processor in a reduced power consumption state. Circuitry is also provided for powering up the processor out of the reduced power consumption state to invalidate data in the cache in order to maintain cache coherency while in the reduced power consumption state.

ADVANTAGE - Allows processor to invalidate individual line of its internal cache while in non-clocked low power state. Does not require additional hardware in computer system, nor require changes to be made to circuit board of computer. Computer system can be upgraded to enhance its performance without changes to the remainder of the system.

Dwg.1/11

Title Terms: INVALID; CACHE ; MEMORY; LOW; POWER; STATE; LOGIC; CIRCUIT; POWER; UP; INTEGRATE; CIRCUIT; REDUCE; POWER; CONSUME; STATE; RUN; INVALID; CYCLE; CACHE ; MEMORY; PLACE; INTEGRATE; CIRCUIT; BACK; REDUCE; POWER; CONSUME; STATE; AFTER; INVALID; CYCLE; COMPLETE

Derwent Class: T01

International Patent Class (Main): G06F-001/32

File Segment: EPI

13/5/18 (Item 16 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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011153292

WPI Acc No: 1997-131216/199712

XRPX Acc No: N97-108357

Power management control method for external cache of computer system and circuit thereof - monitoring CPU and bus state to control chip select or input clock of external cache

Patent Assignee: COMPAL ELECTRONICS INC (COMP-N)

Inventor: GONG S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
TW 291545	A	19961121	TW 94106838	A	19940726	199712 B

Priority Applications (No Type Date): TW 94106838 A 19940726

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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Abstract (Basic): TW 291545 A

The power management control for external **cache** of computer system is mainly based on receiving ADS, M/IQ, HLDA and RDY in the system bus to judge system status and bus utilization.

When the system CPU is not in the bus or I-O period, and the system is not in DMA mode, a **power saving** control signal is generated, controlling the chip **select** line of external **cache**, making it in unselected non-working state.

Title Terms: POWER; MANAGEMENT; CONTROL; METHOD; EXTERNAL; **CACHE** ;
COMPUTER; SYSTEM; CIRCUIT; MONITOR; CPU; BUS; STATE; CONTROL; CHIP;
SELECT; INPUT; CLOCK; EXTERNAL; **CACHE**

Derwent Class: T01

International Patent Class (Main): G06F-001/32

File Segment: EPI

13/5/19 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011013274 **Image available**

WPI Acc No: 1996-510224/199651

XRPX Acc No: N96-430094

Memory device for microprocessor - selects and outputs data, specified by lower order bit of address, from stored data of one line by latch line circuit without reading random access memory

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8263366	A	19961011	JP 9567726	A	19950327	199651 B

Priority Applications (No Type Date): JP 9567726 A 19950327

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 8263366	A	19	G06F-012/04	

Abstract (Basic): JP 8263366 A

The device includes a line latch circuit (120) which stores the data in one line read from a random access memory (116). The data specified by a lower order bit of an address are selected and output from the stored data in one line without reading the RAM.

A branched address (104) or a sequential address relating to an access but not into a same line as the last access in the RAM is selected.

ADVANTAGE - Reduces power consumption to select from line data read during last access and stored to line latch. Enables supplying data and provides access. Enables completing access of cache memory.

Dwg.1/10

Title Terms: MEMORY; DEVICE; MICROPROCESSOR; SELECT; OUTPUT; DATA;
SPECIFIED; LOWER; ORDER; BIT; ADDRESS; STORAGE; DATA; ONE; LINE; LATCH;
LINE; CIRCUIT; READ; RANDOM; ACCESS; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-012/04

International Patent Class (Additional): G06F-009/32

File Segment: EPI

13/5/20 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010988399 **Image available**

WPI Acc No: 1996-485348/199648

Related WPI Acc No: 1999-153183

XRPX Acc No: N96-408926

RISC type microprocessor for desktop and notebook computer - has address bit being predecoded to activate selected segment with groups of instructions being accessed from cache in parallel and stored in register

Patent Assignee: SILICON GRAPHICS INC (SILI-N)

Inventor: KALDANI G G; KOWALCZYK A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5568442	A	19961022	US 9364189	A	19930517	199648 B
			US 95491491	A	19950616	

Priority Applications (No Type Date): US 9364189 A 19930517; US 95491491 A 19950616

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5568442	A	9	G11C-008/00	Cont of application US 9364189

Abstract (Basic): US 5568442 A

The microprocessor includes N **cache** segments organised into X rows and Y columns, a predecoder, and a bus system. Also provided are several X word line drivers, N row decoders, a staging register, and a K:1 multiplexer. The **cache** segments have a subset of the Y columns included in the **cache** and X segmented word lines. The predecoder receives a portion of a unique index field and has outputs coupled to N segment select lines.

Each predecoder, corresponding to one **cache** segment, decodes the first portion to assert a select signal on one segment select line identified by this portion. The amp/write **units** couple each **cache** segment to the bus and each have an input coupled to a **select line**. Each row decoder decodes the second **portion** of the index **field** to **activate** an X word **line** driver when a **select** signal is asserted. The staging register receives a group of K data words, group length being Y/N bits, from the segment when a select signal is asserted. The multiplexer receives a third portion of the index field and decodes this portion to select one of the K data words.

USE/ADVANTAGE - For portable computing device. Segmented **cache** reduces word line loading to reduce **power consumption** and increase speed. Reduced number of **cache** accesses, e.g. by factor of two, during sequential instruction execution as stored instructions are fetched from register. Provides high performance advantages of RISC design with reduced cost and power dissipation.

Dwg. 5/5

Table Terms: TYPE; MICROPROCESSOR; COMPUTER; ADDRESS; BIT; ACTIVATE; SELECT ; SEGMENT; GROUP; INSTRUCTION; ACCESS; **CACHE** ; PARALLEL; STORAGE; REGISTER

Index Terms/Additional Words: REDUCED; INSTRUCTION; SET; COMPUTER; COMPLEX; INSTRUCTION; SET; COMPUTER

Derwent Class: U14

International Patent Class (Main): G11C-008/00

File Segment: EPI

13/5/21 (Item 19 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010928101 **Image available**

WPI Acc No: 1996-425052/199642

XRPX Acc No: N96-357916

Power saving **architecture** for cache memory - has decoder/driver **assembly which selects exclusively either first or second array, and electrically activating one of wordlines in selected array in accordance with address signal**

Patent Assignee: INTEL CORP (ITLC)

Inventor: DIMARCO D P; HOSE R K

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5555529	A	19960910	US 93174382	A	19931228	199642 B
			US 95542514	A	19951013	

Priority Applications (No Type Date): US 93174382 A 19931228; US 95542514 A 19951013

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5555529	A	8	G11C-007/00	Cont of application US 93174382

Abstract (Basic): US 5555529 A

The system includes a first memory array with memory cells for storing digital data. A second memory array has memory cells that stores digital data. A single wordline address decoder/driver assembly for receives an address signal from the CPU. The decoder/driver assembly has device for selecting exclusively either the first or the second array, and electrically **activating** one of the wordlines in the **selected** array in accordance with the address signal. Each bit line column intersected by the electrically **activated** word- line electrically discharges to provide the value of the memory cell at the point of intersection. Each bit line column intersected by the unactivated corresponding wordline does not electrically discharge to provide the value of the memory cell, thereby reducing **power consumption** of the memory.

ADVANTAGE - Reduces average current for read operation significantly. Provides improved **cache** memory architecture in computer system.

Dwg.3/3

Title Terms: POWER; SAVE; ARCHITECTURE; **CACHE** ; MEMORY; DECODE; DRIVE; ASSEMBLE; SELECT; EXCLUDE; FIRST; SECOND; ARRAY; ELECTRIC; ACTIVATE; ONE; SELECT; ARRAY; ACCORD; ADDRESS; SIGNAL

Derwent Class: T01; U13; U14

International Patent Class (Main): G11C-007/00

International Patent Class (Additional): G11C-008/00

File Segment: EPI

13/5/22 (Item 20 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010746346 **Image available**

WPI Acc No: 1996-243301/199625

XRPX Acc No: N96-203970

Semiconductor memory e.g cache memory for microprocessor - has interruption elements that interrupt through- current flowing through selected coil, during reset

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8095859	A	19960412	JP 94233713	A	19940928	199625 B

Priority Applications (No Type Date): JP 94233713 A 19940928

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 8095859	A	7	G06F-012/08	

Abstract (Basic): JP 8095859 A

The semiconductor memory has a cell (1) connected in each intersection position of a bit line (103-1) and a word line (102-1) which is arranged in the shape of a matrix. The word line is used to select a predetermined cell. The bit line is used to perform read/write operation on the selected cell.

A reset **element** (5) is used to reset the **specific** cell which is connected in the direction of the bit line . During reset, the through- **current** in that cell is interrupted using a pair of through-current interruption elements (3,13).

ADVANTAGE - Reduces time taken for reset. Reduces power consumption .

Dwg.1/6

Title Terms: SEMICONDUCTOR; MEMORY; **CACHE** ; MEMORY; MICROPROCESSOR; INTERRUPT; ELEMENT; INTERRUPT; THROUGH; CURRENT; FLOW; THROUGH; SELECT; WAIT; RESET

Derwent Class: T01

International Patent Class (Main): G06F-012/08

File Segment: EPI

13/5/23 (Item 21 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010173579 **Image available**

WPI Acc No: 1995-074832/199510

Related WPI Acc No: 1997-099756; 1999-142273

XREF Acc No: N95-059334

Synchronous semiconductor memory esp. DRAM with refresh - has memory cell array divided into banks, each with respective read and write registers and has read or write operation only to banks designated by external bank addresses

Patent Assignee: MITSUBISHI DENKI KK (MITQ)

Inventor: IWAMOTO H; KAJIMOTO T; KONISHI Y; MIYAMOTO T

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5384745	A	19950124	US 9346333	A	19930414	199510 B

Priority Applications (No Type Date): JP 92155026 A 19920615; JP 92107424 A 19920427

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5384745	A	90	G11C-008/00	

Abstract (Basic): US 5384745 A

The semiconductor memory has control signals, external signals including address signals having bank addresses and data input synchronised with an external clock signal e.g. a system clock. The memory includes a cell array divided into banks operated independent from each other. There are read data storing registers and write data storing registers operating **independent** from each other, corresp. to the **banks** . The memory **banks** are **activated** for memory cell selection **independent** from each other in accordance with the **bank** addresses, which designate individual banks.

A data read or write operation is performed only for the bank designated by the bank addresses. Pref. data input/output setting circuitry and bank number setting circuitry, responding to information from the data input/output number set, respectively set the number of data which can be input or output at one time and set an upper limit on the number of banks.

USE/ADVANTAGE - Implements processor system without **cache** memory. Small area, high speed of operation, low **power consumption** ; multiple functions.

Dwg.1/69

Title Terms: SYNCHRONOUS; SEMICONDUCTOR; MEMORY; DRAM; REFRESH; MEMORY; CELL; ARRAY; DIVIDE; BANK; RESPECTIVE; READ; WRITING; REGISTER; READ; WRITING; OPERATE; BANK; DESIGNATED; EXTERNAL; BANK; ADDRESS

Derwent Class: U14

International Patent Class (Main): G11C-008/00

File Segment: EPI

13/5/24 (Item 22 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009475703 **Image available**

WPI Acc No: 1993-169238/1 321
XRPX Acc No: N93-129578

Data processing system including modular memory system - stores particular data in cache memory of one module and non-volatile memory of another module with separate power supply for each module .

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: HARTUNG M H; SINGH S; WADE F L

Number of Countries: 006 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 543582	A1	19930526	EP 92310401	A	19921113	199321 B
CA 2072728	A	19930521	CA 2072728	A	19920629	199332
EP 543582	B1	19950816	EP 92310401	A	19921113	199537
DE 69204143	E	19950921	DE 604143	A	19921113	199543
			EP 92310401	A	19921113	
KR 9601947	B1	19960208	KR 9220907	A	19921109	199908

Priority Applications (No Type Date): US 91795215 A 19911120

Cited Patents: 1.Jnl.Ref; DE 3311881

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 543582	A1	E	4	G06F-011/20	
Designated States (Regional): DE FR GB IT					
EP 543582	B1	E	5	G06F-011/20	
Designated States (Regional): DE FR GB IT					
DE 69204143	E			G06F-011/20	Based on patent EP 543582
CA 2072728	A			G06F-012/16	
KR 9601947	B1			G06F-012/16	

Abstract (Basic): EP 543582 A

The memory system includes a number of split memory modules for storing data in first and second sections. The first sections of the memory modules comprise a **cache** memory and the second sections comprise a non-volatile memory. A number of **power** supplies are **used**, each for supplying **power** to one of the memory modules.

The same data is stored in the first section of one of the memory **modules** and the second **section** of another of the **modules**. Each **power** supply is coupled to a **separate cache** memory and non-volatile memory. A transfer mechanism couples addresses and data to or from a source in parallel to one of the **cache** memories and one of the non-volatile memories not connected to the same power supply.

ADVANTAGE - By storing data in both **sections** of different **modules**, **powered** from **separate** sources, loss of data is avoided.

Dwg.1/2

Title Terms: DATA; PROCESS; SYSTEM; MODULE; MEMORY; SYSTEM; STORAGE; DATA; **CACHE**; MEMORY; ONE; MODULE; NON; VOLATILE; MEMORY; MODULE; SEPARATE; POWER; SUPPLY; MODULE

Derwent Class: T01; U14

International Patent Class (Main): G06F-011/20; G06F-012/16

International Patent Class (Additional): G06F-001/26; G11C-005/14

File Segment: EPI

13/5/25 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

008711344 **Image available**
WPI Acc No: 1991-215365/199129
XRPX Acc No: N91-164382

Set associative cache memory for microprocessor - includes memory arrays arranged in group for each line and only memory array selected is made operative reducing power consumption

Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)

Inventor: YAMAGUCHI S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
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Priority Applications (No Type Date): JP 88198209 A 19880809

Abstract (Basic): US 5029126 A

In the **cache** memory, the set associative type having m sets (m is an integer and m is greater than 1) is adopted. The **cache** memory comprises n lines (n is a power of two and n is greater than 1) per block and n memory array areas in each of which one word is formed of $m \times k$ bits, where k is the number of bits in one per line, block and set. A memory array area, which is made operative when the **cache** memory is accessed, is limited to only one by an address which selects an offset address line.

Even in the case of a **cache** memory having an odd number of sets, since the memory array is composed for every line and this makes it possible to use the memory array as an even number of memory array areas, the layout design and the floor plan of a semiconductor integrated circuit to be used therein can be made easy and a chip space can be effectively utilised.

USE/ADVANTAGE - Microprocessor needing large capacity **cache** memory. reduces space voltage by dividing memory array into even number of sets. (Odd number wastes space). (4pp Dwg.No.1/1)'

Title Terms: SET; ASSOCIATE; **CACHE** ; MEMORY; MICROPROCESSOR; MEMORY; ARRAY ; ARRANGE; GROUP; LINE; MEMORY; ARRAY; SELECT; MADE; OPERATE; REDUCE; POWER; CONSUME

Derwent Class: T01; U14

International Patent Class (Additional): G11C-011/40; G11C-015/00

File Segment: EPI

16/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

07668588 **Image available**
LOW POWER - CONSUMPTION CACHE MEMORY DEVICE

PUB. NO.: 2003-162448 [JP 2003162448 A]
PUBLISHED: June 06, 2003 (20030606)
INVENTOR(s): TOKUNAGA YUICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 2001-360582 [JP 2001360582]
FILED: November 27, 2001 (20011127)
INTL CLASS: G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To **inactively** read a **cache line** even if it has a large **cache line** size, by restricting the divided number of memory to a minimum in a set associative type **cache** memory.

SOLUTION: The cache memory has plural **ways** 21, 22, 31 and 32. When a cache-hit occurs, a cache control circuit 1, expecting successive access, considers succeeding addresses from the plural ways via comparators 51 and 52, and selects data from the way at a corresponding address side. The cache memory is divided into bank memories as storing/reading divisions. Preceding bank memories 311 and 321 have smaller sizes, and succeeding bank memories 312 and 322 have larger sizes, each including latch circuit for latching memory information of the succeeding bank memory. The cache control circuit 1 is adapted to read out the information in the latch circuit of the succeeding bank memory when reading for successive addresses does not change the way.

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16/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

00527954 **Image available**
CACHE MEMORY DEVICE AND METHOD FOR CONTROLLING CACHE MEMORY DEVICE

PUB. NO.: 2000-113677 [JP 2000113677 A]
PUBLISHED: April 21, 2000 (20000421)
INVENTOR(s): YAMADA KAZUYUKI
APPLICANT(s): NEC CORP
APPL. NO.: 10-281726 [JP 98281726]
FILED: October 02, 1998 (19981002)
INTL CLASS: G11C-011/41; G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To reduce average **power consumption** during the data writing to a memory by comparing, when data writing operation is executed to the memory, the latest data content read from the memory with the data to be written and then executing the write operation for the **part** in which data content is changed.

SOLUTION: A **cache** memory 31 is provided with BE(bit enable) signal 43 and the SRAM input/output **part** is activated or **deactivated** in every bit with the BE signal 43 to control the operation permitted or non-permitted. For this purpose, the latest read data from the **cache** memory 31 is stored in the data input/output flip-flop(F/F) 32 and conformity between the output of F/F 32 and the data 46 to be written into the cache memory 31 is determined with a 2-input exclusive OR gate. The BE signal 43 is generate from each bit of the output 44 of gate 34 and chip enable signal CE 23 from the controller 4 with the 2-input logical OR gate 33.

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16/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

0419467 **Image available**
INFORMATION PROCESSOR

PUB. NO.: 09-034787 [JP 9034787 A]
PUBLISHED: February 07, 1997 (19970207)
INVENTOR(s): SATO MAKOTO
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 07-205089 [JP 95205089]
FILED: July 20, 1995 (19950720)
INTL CLASS: [6] G06F-012/08; G06F-012/08; G06F-001/32
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.9
(INFORMATION PROCESSING -- Other)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce **power consumption** without lowering performance by controlling a cache memory sub-system into an inactive state when any input operation is not detected for prescribed time by a monitoring means.

SOLUTION: An inactive state detection **part** (monitoring means) 4 monitors the input operation at all times. When the input operation is not detected for the prescribed time by the **inactive** state detection **part** 4, a CPU 8 controls a **cache** memory sub-system 7 into the **inactive** state. Thus, when the **inactive** state detection **part** 4 does not detect any input operation signal for the prescribed time, an interrupt signal is generated and corresponding to the generation of this interrupt signal, the CPU 8 controls cache memories 9 and 9' more than one into the inactive state at least and inhibits the electrification to those cache memories 9 and 9'. Thus, **power consumption** can be reduced without lowering performance.

16/5/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015441585 **Image available**
WPI Acc No: 2003-503727/200347
XRPX Acc No: N03-399892

Front-end unit for processor, has instruction cache system whose output is coupled to segment builder that is selectively disabled by access filter coupled to input of cache system

Patent Assignee: RONEN R (RONE-I); SOLOMON B (SOLO-I)

Inventor: RONEN R; SOLOMON B

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030061469	A1	20030327	US 2001961202	A	20010924	200347 B

Priority Applications (No Type Date): US 2001961202 A 20010924

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030061469	A1	10	G06F-009/30	

Abstract (Basic): US 20030061469 A1

NOVELTY - An instruction **cache** system has an input for new addresses and an output for decoded instructions. A **segment** builder having an input coupled to the **cache** system's output, is **disabled** selectively by an access filter coupled to the **cache** system's input. A **segment cache** is coupled to the **segment** builder.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

- (1) cache hit control method;
- (2) cache; and
- (3) access filter.

USE - Front-end unit for processor.

ADVANTAGE - The access filter selectively enables or disables segment builders within the front-end, to ensure that only instruction segments that are likely to be reused by program flow is stored in the segment cache, thereby achieving power conservation.

DESCRIPTION OF DRAWING(S) - The figure shows the processor conservation method.

pp; 10 DwgNo 4/7

Title Terms: FRONT; END; UNIT; PROCESSOR; INSTRUCTION; CACHE; SYSTEM;
OUTPUT; COUPLE; SEGMENT; BUILD; SELECT; DISABLE; ACCESS; FILTER; COUPLE;
INPUT; CACHE; SYSTEM

Derwent Class: T01

International Patent Class (Main): G06F-009/30

File Segment: EPI

16/5/5 (Item 2 from file: 350)

DIALOG(R) File 350: Derwent WPIX

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015280309 **Image available**

WPI Acc No: 2003-341240/200332

XRPX Acc No: N03-272947

Cache meta data storage method in computer, involves storing meta data corresponding to stored cache data, in partitioned section of cache memory

Patent Assignee: COULSON R L (COUL-I); GRIMSRUD K S (GRIM-I); ROYER R J (ROYE-I); INTEL CORP (ITLC)

Inventor: COULSON R L; GRIMSRUD K S; ROYER R J; COULSON R; GRIMSRUD K; ROYER R

Number of Countries: 100 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030005219	A1	20030102	US 2001895578	A	20010629	200332 B
WO 200303217	A2	20030109	WO 2002US19787	A	20020620	200332

Priority Applications (No Type Date): US 2001895578 A 20010629

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030005219	A1		9 G06F-012/00	
WO 200303217	A2 E		G06F-012/00	

US 20030005219 A1

WO 200303217 A2 E

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20030005219 A1

NOVELTY - The cache memory (150) is partitioned and data is stored in partitioned sections of memory. The meta data corresponding to the stored cache data, is stored in another partitioned section of the cache memory..

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) non-volatile memory;
- (2) cache meta data storing system;
- (3) cache meta data storing program; and
- (4) system boot.

USE - For storing cache meta data in computer.

ADVANTAGE - The cache state is preserved during power failure or normal system shut - down condition, by storing meta data and the cache data in the partitioned sections of cache memory, thus improves system performance. The initialization time for a cache

memory is reduced significantly.

DESCRIPTION OF DRAWING(S) - The figure shows an exemplary system explaining the cache meta data storage method.

cache memory (150)

pp; 9 DwgNo 1/3

Title Terms: CACHE; META; DATA; STORAGE; METHOD; COMPUTER; STORAGE; META;
DATA; CORRESPOND; STORAGE; CACHE; DATA; PARTITION; SECTION; CACHE; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

16/5/6 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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015242657 **Image available**

WPI Acc No: 2003-303583/200330

XRPX Acc No: N03-241450

Secondary battery charging state checking method for portable telephone set, involves detecting current consumed by all circuits during which command cache is disabled, for preventing memory from entering stand by mode

Patent Assignee: NIPPONDENSO CO LTD (NPDE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002171686	A	20020614	JP 2000371321	A	20001206	200330 B

Priority Applications (No Type Date): JP 2000371321 A 20001206

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

JP 2002171686 A 6 H02J-007/10

Abstract (Basic): JP 2002171686 A

NOVELTY - The current consumed by all the circuits is detected by the central processing unit (CPU) using an analog-to-digital converter, for checking the charged state of the secondary battery. The command **cache** is **disabled** during the detection to prevent the flash read only memory (ROM) storing a control program from entering standby mode.

USE - For portable telephone set.

ADVANTAGE - Accurately checks the charging state of the battery **used** as the secondary **power** source using the central processing unit (CPU).

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining the battery charging state checking method. (Drawing includes non-English language text).

pp; 6 DwgNo 1/1

Title Terms: SECONDARY; BATTERY; CHARGE; STATE; CHECK; METHOD; PORTABLE;
TELEPHONE; SET; DETECT; CURRENT; CONSUME; CIRCUIT; COMMAND; CACHE;
DISABLE; PREVENT; MEMORY; ENTER; STAND; MODE

Derwent Class: W01; W02; X16

International Patent Class (Main): H02J-007/10

International Patent Class (Additional): H04B-007/26; H04M-001/725

File Segment: EPI

16/5/7 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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015206599 **Image available**

WPI Acc No: 2003-267135/200326

XRPX Acc No: N03-212319

Front end processing system for mobile computing application, has instruction processing system whose enable control input is coupled to hit/miss output of UOP cache connected to instruction cache

Patent Assignee: ORENSTIEN D (OREN-I); RONEN R (RONE-I); SOLOMON B (SOLO-I)

Inventor: ORENSTIEN D; RONEN R; SOLOMON B

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030009620	A1	20030109	US 2001892566	A	20010628	200326 B

Priority Applications (No Type Date): US 2001892566 A 20010628

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030009620	A1	11	G06F-012/00	

Abstract (Basic): US 20030009620 A1

NOVELTY - The system has a UOP cache (240) and an instruction cache (210) inputs which are coupled to a common addressing input. An instruction processing system comprising instruction synchronizer (220) and an instruction decoder (230), is in communication with the instruction cache, and has an enabling control input coupled to the hit/miss output of the UOP cache

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for cache.

USE - For execution of program in processors used in mobile computing applications.

ADVANTAGE - The instruction processing system enables and disables internal circuits of processor based on output received from UOP cache, thereby the power consumed by front end unit of processor is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of front end unit of processor.

Instruction cache (210)
instruction synchronizer (220)
instruction decoder (230)
UOP cache (240)
pp; 11 DwgNo 3/8

Title Terms: FRONT; END; PROCESS; SYSTEM; MOBILE; COMPUTATION; APPLY;

INSTRUCTION; PROCESS; SYSTEM; ENABLE; CONTROL; INPUT; COUPLE; HIT; MISS; OUTPUT; CACHE; CONNECT; INSTRUCTION; CACHE

Derwent Class: T01; U14

International Patent Class (Main): G06F-012/00

File Segment: EPI

16/5/8 (Item 5 from file: 350)

DIALOG(R) File 350: Derwent WPIX

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014660996

WPI Acc No: 2002-481700/200252

XRFX Acc No: N02-380532

Data or image processor has an instruction cache consisting of a number of cache memory units of which only those storing demanded instructions are enabled and powered at any one time

Patent Assignee: FUJITSU LTD (FUIT)

Inventor: SATOH T; UTSUMI H; YAMAZAKI Y; YODA H

Number of Countries: 030 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1217502	A1	20020626	EP 2001310811	A	20011221	200252 B
US 20020080662	A1	20020627	US 200123905	A	20011221	200252
JP 2002196981	A	20020712	JP 2000391369	A	20001222	200261
CN 1367428	A	20020904	CN 2001145765	A	20011221	200281
KR 2002051874	A	20020629	KR 200182560	A	20011221	200301

Priority Applications (No Type Date): JP 2000391369 A 20001222

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 1217502	A1 E	20	G06F-001/32	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR

US 20020080662 A1 G11C-007/00
JP 2002196981 A 15 G06F-012/08
CN 1367428 A G06F-009/00
KR 2002051874 A G06F-009/32

Abstract (Basic): EP 1217502 A1

NOVELTY - When the first instruction of a **block** is read all instruction **cache** memory **units** are enabled. However, when the first instruction of the new **block** is read into a **cache** memory **unit** all the other **cache** memory **units** are **disabled** while subsequent instructions in the **block** are read into the same **cache** memory **unit**. When retrieving instructions from the instruction **cache** a hit in one of the memory **units** is used to **disable** all the other **units**. The instruction **cache** may be provided by memory external to the processor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for

(a) a system comprising a processor and an external instruction cache memory

(b) and a controlling method for an instruction cache

USE - In data processors.

ADVANTAGE - Reduces **power** **consumption** by **disabling** unwanted instruction **cache** memory **units**.

pp; 20.DwgNo 0/12

Title Terms: DATA; IMAGE; PROCESSOR; INSTRUCTION; CACHE; CONSIST; NUMBER; CACHE; MEMORY; UNIT; STORAGE; DEMAND; INSTRUCTION; ENABLE; POWER; ONE; TIME

Derwent Class: T01; U14

International Patent Class (Main): G06F-001/32; G06F-009/00; G06F-009/32; G06F-012/08; G11C-007/00

International Patent Class (Additional): G06F-012/00; G06F-013/00; G06F-015/00

File Segment: EPI

16/5/9 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012804308 **Image available**

WPI Acc No: 1999-610538/199952

WPIX Acc No: N99-449854

Power consumption reduction method in non-blocking cache of notebook computer

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); MOTOROLA INC (MOTI)

Inventor: KUTTANNA B M; PATEL R B

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5974505	A	19991026	US 97927131	A	19970902	199952 B

Priority Applications (No Type Date): US 97927131 A 19970902

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5974505	A	10	G06F-013/16	

Abstract (Basic): US 5974505 A

NOVELTY - In response to a cache request, it is determined whether the request information matches with a linefill information in the cache memory during ongoing linefill operation. When a match with linefill information is determined, an index matching bit is set and the clock to the **cache** memory and **tag** of the **cache** are temporarily **disabled**.

DETAILED DESCRIPTION - When the determination results in a mismatch, the cache request matching determination is performed after completion of the ongoing linefill operation. The index matching bit of the cache memory is reset when a doubleword is received. An INDEPENDENT CLAIM is also included for **power** **consumption** reduction mechanism in cache memory.

USE - For reducing power consumption of non-blocking cache in notebook computers.

ADVANTAGE - Since the clocks to the tag and cache data arrays are turned off immediately when one of the index matching bit is asserted, unnecessary tag lookups and unnecessary power dissipation from the cache is avoided. By reducing clock signal transition from section 's local clock generators to a zero frequency, power consumption is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart for power consumption reducing procedure in non-blocking cache in a notebook computer.

pp; 10 DwgNo 4/5

Title Terms: POWER; CONSUME; REDUCE; METHOD; NON; BLOCK; CACHE; COMPUTER

Derwent Class: T01

International Patent Class (Main): G06F-013/16

File Segment: EPI

16/5/10 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012523059 **Image available**

WPI Acc No: 1999-329165/199928

Related WPI Acc No: 1999-329162; 1999-329163; 1999-431815; 1999-481199

XRFX Acc No: N99-247051

Cache memory architecture with power consumption control

Patent Assignee: TEXAS INSTR FRANCE (TEXI); TEXAS INSTR INC (TEXI)

Inventor: CHAUVEL G; D'INVERNO D; LASSERRE S

Number of Countries: 026 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 921471	A1	19990609	EP 98401530	A	19980622	199928 B
JP 2000172561	A	20000623	JP 98377025	A	19981207	200036 N

Priority Applications (No Type Date): EP 97402958 A 19971205; JP 98377025 A 19981207

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 921471 A1 E 10 G06F-012/08

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT

LI LT LU LV MC MK NL PT RO SE SI

JP 2000172561 A 28 G06F-012/08

Abstract (Basic): EP 921471 A1

NOVELTY - The same data line in the cache may be hit multiple times in succession, and the cache look-up circuit is by-passed when the data is available in the output buffer associated with the cache memory.

DETAILED DESCRIPTION - A cache controller (52) has an internal register for storing the address of an active line currently latched in an output buffer of the high speed cache data array (56) which stores the cached data values from the main memory. If a memory access request specifies an address which would be contained in the active line, the cache look-up mechanisms in the tag array (54) and the data array (56) are disabled, and the data is taken from the output buffer. An INDEPENDENT CLAIM is included for; a cache memory circuit; a processing device having a cache memory.

USE - High speed, low power cache memory, e.g. associative cache, for use in mobile electronic devices e.g. mobile phone or smart-phone.

ADVANTAGE - Reduces power consumed by the cache circuitry, and increases the speed of data retrieval allowing greater processor speed.

DESCRIPTION OF DRAWING(S) - The drawing is a block diagram of a cache architecture for use in a mobile electronic device.

Cache memory architecture (50)

Cache controller (52)

Tag array (54)

Data array (56)

pp; 10 DwgNo 3/4

Title Terms: CACHE; MEMO; ARCHITECTURE; POWER; CONSUME; CONTROL
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

16/5/11 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012193648 **Image available**
WPI Acc No: 1998-610561/199851
XRPX Acc No: N98-474881

Cache coherency maintenance for processors in powered down modes - has
clock spine feeding sets of functional circuits and separate clock
enables to power cache circuit selectively when needed

Patent Assignee: INTEL CORP (ITLC)
Inventor: CHUNG C; EAKAMBARAM R; HORIGAN J; KARDACH J P; NAKANISHI T; SENYK
E S

Number of Countries: 082 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9850846	A1	19981112	WO 98US1519	A	19980127	199851 B
AU 9862507	A	19981127	AU 9862507	A	19980127	199915
US 6014751	A	20000111	US 97841858	A	19970505	200010
TW 414875	A	20001211	TW 98101803	A	19980210	200124
JP 2002510413	W	20020402	JP 98548035	A	19980127	200225
			WO 98US1519	A	19980127	

Priority Applications (No Type Date): US 97841858 A 19970505

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 9850846 A1 E 37 G06F-001/18
Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ
DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS
LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR
TT UA UG UZ VN YU ZW

Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GM GR IE
IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9862507 A G06F-001/18 Based on patent WO 9850846
US 6014751 A G06F-001/10
TW 414875 A G06F-001/28
JP 2002510413 W 46 G06F-012/08 Based on patent WO 9850846

Abstract (Basic): WO 9850846 A

The integrated circuit, e.g. a processor in a multiprocessor system
has multiple power down modes. The processor (14) has a number of core
functional units, e.g. FPU (50), ALU (53) and prefetch logic (34). It
also has a second set of functional units related to cache control,
e.g. data (51) and code (38) caches and a bus interface (32). A central
clock spine (150) feeds all of the units via selection gates (143,144).

A stop grant circuit (117) can **disable** (141) one set of **units**
to reduce power but leaving the **cache** circuits operating. A quick
start circuit (116) can **disable** (142) **cache** circuits but rapidly
re-enable them on bus accesses.

ADVANTAGE - Reduces **power consumption** while enabling cache
coherency and snoop circuits to operate when needed.

Dwg.5/12

Title Terms: CACHE; COHERE; MAINTAIN; PROCESSOR; POWER; DOWN; MODE; CLOCK;
SPINE; FEED; SET; FUNCTION; CIRCUIT; SEPARATE; CLOCK; ENABLE; POWER;
CACHE; CIRCUIT; SELECT; NEED

Derwent Class: T01

International Patent Class (Main): G06F-001/10; G06F-001/18; G06F-001/28;
G06F-012/08

International Patent Class (Additional): G06F-001/04

File Segment: EPI

16/5/12 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012010540 **Image available**

WPI Acc No: 1998-427450/199836

XRPX Acc No: N98-333676

Power consumption control method for computer system - involves
stopping power supply to device driver and processor after storing data
regarding their operating state in memory

Patent Assignee: MICROSOFT CORP (MICR-N)

Inventor: KENERIS K S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5784628	A	19980721	US 96614186	A	19960312	199836 B

Priority Applications (No Type Date): US 96614186 A 19960312

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5784628	A		17	G06F-001/26	

Abstract (Basic): US 5784628 A

The method involves detecting the power down condition that indicates the need for suspension of computer system. Then, the possibility for suspension of computer system is verified.

The data regarding state of the device driver and a processor is stored in the memory. Then, the power supply to the device driver and processor is stopped.

ADVANTAGE - Enables formation of software controlled power control unit in computer. Offers standard user interface to control power state of computer. Enables effective prediction of power management actions. Facilitates delayed switch OFF of disk drive motor until disk cache is flushed.

Dwg.4/8

Title Terms: POWER; CONSUME; CONTROL; METHOD; COMPUTER; SYSTEM; STOP; POWER
; SUPPLY; DEVICE; DRIVE; PROCESSOR; AFTER; STORAGE; DATA; OPERATE; STATE;
MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-001/26

International Patent Class (Additional): G06F-001/32

File Segment: EPI

16/5/13 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

011819187 **Image available**

WPI Acc No: 1998-236097/199821

XRPX Acc No: N98-187210

Notebook computer system with power save function - in which cache
memory is set up in disable state for predefined time after it is
switched to normal mode, for predetermined time

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: ANDO M

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10074167	A	19980317	JP 96230155	A	19960830	199821 B
US 5931951	A	19990803	US 97917599	A	19970826	199937

Priority Applications (No Type Date): JP 96230155 A 19960830

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10074167	A		19	G06F-012/08	
US 5931951	A			G06F-001/32	

Abstract (Basic): JP 100 67 A

The system includes a CPU (11). When the CPU is switched to **power save** mode from normal mode, a controller (12) switches a cache memory (14) to the **power save** mode by supplying **power** down signal to the cache memory.

When the CPU is switched to normal mode, the **cache** memory is switched to the normal mode and is set up in the **disable** state by a **disable** unit for a predefined time before it is switched to the **power save** mode. The **cache** memory is switched to the enable state by an enable unit after the predefined time elapses and the access of cache memory is continued.

ADVANTAGE - Realizes reduced **power** consumption to high performance. Prevents malfunction resulting from access of cache memory in normal mode.

Dwg.1/15

Title Terms: COMPUTER; SYSTEM; POWER; SAVE; FUNCTION; CACHE; MEMORY; SET; UP; DISABLE; STATE; PREDEFINED; TIME; AFTER; SWITCH; NORMAL; MODE; PREDETERMINED; TIME

Derwent Class: T01

International Patent Class (Main): G06F-001/32; G06F-012/08

International Patent Class (Additional): G06F-001/26

File Segment: EPI

16/5/14 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010083220 **Image available**

WPI Acc No: 1994-350933/199444

XRPX Acc No: N94-275365

Architecture for fully integrated cache - has cache memory in data and access information sections where data section can be disabled and word lines formed to protect data from noise

Patent Assignee: INT BUSINESS MACHINES CORP (IBM); IBM CORP (IBM)

Inventor: DAVIS A; MILTON D W

Number of Countries: 007 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 624844	A2	19941117	EP 94103887	A	19940314	199444 B
EP 624844	A3	19941214	EP 94103887	A	19940314	199537
US 5640339	A	19970617	US 9360776	A	19930511	199730
			US 96662890	A	19960311	
CN 1106951	A	19950816	CN 94104365	A	19940419	199731
US 5717648	A	19980210	US 9360776	A	19930511	199813
			US 95473158	A	19950607	
US 5727180	A	19980310	US 9360776	A	19930511	199817
			US 95473159	A	19950607	
JP 10232836	A	19980902	JP 9465905	A	19940404	199845
			JP 97283617	A	19940404	
JP 10232837	A	19980902	JP 9465905	A	19940404	199845
			JP 97283797	A	19940404	
KR 9616403	B1	19961211	KR 948379	A	19940419	199931
JP 3277145	B2	20020422	JP 9465905	A	19940404	200234
			JP 97283797	A	19940404	

Priority Applications (No Type Date): US 9360776 A 19930511; US 96662890 A 19960311; US 95473158 A 19950607; US 95473159 A 19950607

Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 352806

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 624844 A2 E 23 G06F-012/08

Designated States (Regional): DE FR GB

EP 624844 A3 G06F-012/08

US 5640339 A 18 G11C-007/00 Cont of application US 9360776

CN 1106951 A G11C-015/00

US 5717648 A 19 G11C-007/00 Div ex application US 9360776

US 5727180 A 19 G06F-012/00 Div ex application US 9360776

JP 10232836	A	18 G-012/08	Div ex application J 465905
JP 10232837	A	19 G06F-012/08	Div ex application JP 9465905
KR 9616403	B1	G06F-012/08	
JP 3277145	B2	18 G06F-012/08	Div ex application JP 9465905
			Previous Publ. patent JP 10232837

Abstract (Basic): EP 624844 A

The fully integrated cache architecture includes a layout to protect against noise. The cache (41) includes a storage array holding DATA, TAG, VALID and LRUA bits. The array is formed with these elements on a single word line. The tags supplied are compared with stored tags by comparators (CA..CD). The LRU control (150) uses this and the validity bits to update the LRUA data bits.

The tag information is received before the data information due to the layout. This allows some areas of the array to be disabled to **save power**. The metal connection layer protects data from noise.

USE/ADVANTAGE - High noise immunity, full support of integrated validity/LRU cache write mode. Provides power reduction, with true LRU update procedure and simple structure without increased access time.

Dwg.3/15

Title Terms: ARCHITECTURE; INTEGRATE; CACHE; CACHE; MEMORY; DATA; ACCESS; INFORMATION; SECTION; DATA; SECTION; CAN; DISABLE; WORD; LINE; FORMING; PROTECT; DATA; NOISE

Derwent Class: T01

International Patent Class (Main): G06F-012/00; G06F-012/08; G11C-007/00; G11C-015/00

International Patent Class (Additional): G06F-012/12; G06F-013/00; G11C-008/00; G11C-011/41; G11C-015/04

File Segment: EPI

File 348:EUROPEAN PATENT 1978-2004/Feb W05

(c) 2004 European Patent Office

File 349:PCT FULLTEXT 1979-2002/UB=20040304,UT=20040226

(c) 2004 WIPO/Univention

Set	Items	Description
S1	25912	CACHE? ? OR CACHING
S2	309976	(POWER??? OR SHUT????) (3W)DOWN OR POWERDOWN OR SHUTDOWN OR SHUTTINGDOWN OR DISABL??? OR DEACTIVAT? OR DE()ACTIVAT? OR INACTIVE OR INACTIVAT? OR (TURN??? OR SWITCH??? OR FLIP???? OR TOGGL???) (3W)OFF OR INOPERAT? OR DISENGAG?
S3	1515010	INDIVIDUAL? OR INDEPENDENT? OR SEPARATE OR SEPARATELY OR PARTICULAR OR SELECTED OR SELECT OR SELECTIV? OR SPECIFIC OR CERTAIN
S4	12253	S2(7N)S3(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SEGMENT? ? OR CONSTITUENT? ?)
S5	1093650	POWER??? OR POWERUP OR ENABL??? OR ACTIVAT? OR (TURN??? OR SWITCH??? OR FLIP???? OR TOGGL???) (3W)ON OR ENGAG??? OR ELECTRICITY OR CURRENT
S6	94844	S3(7N)S5(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SUBCOMPONENT? ? OR CONSTITUENT? ?)
S7	100512	(POWER OR ELECTRICITY) (3N) (CONSUMPTION OR CONSUMED OR CONSUME OR CONSUMES OR CONSUMING OR USE OR USED OR USAGE OR EXPENDITURE? ? OR SAV??? OR CONSERV? OR UTILIZ? OR UTILIS? OR PRESERV? OR SPENT OR SPENDING)
S8	107	S1(50N)S4
S9	14	S1(100N)S4(100N)S7
S10	413	S1(20N)S6
S11	33	S10(100N)S7
S12	25	S11 NOT S9
S13	650	S1(15N)S2(15N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SEGMENT? ? OR CONSTITUENT? ?)
	42	S7(100N)S13
	33	S14 NOT (S9 OR S12)

9/3,K/1 (Item 1 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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01135871

Digital signal processor

Digitaler Signalprozessor

Processeur de signaux numeriques

PATENT ASSIGNEE:

TEXAS INSTRUMENTS INC., (279076), 13500 North Central Expressway, Dallas,
Texas 75243, US\ (Applicant designated states: , BE; CH; DE; DK; ES; FI;
GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; AT; CY)

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Rosenzweig, Jack, 1210 Macon Avenue, Pittsburgh, PA 15218, (US)

LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 992916 A1 000412 (Basic)

APPLICATION (CC, No, Date): EP 98402455 981006;

DESIGNATED STATES: DE; FI; FR; GB; SE

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06F-015/78; G06F-009/38

ABSTRACT WORD COUNT: 221

NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text Language Update Word Count

CLAIMS A (English)	200015	494
SPEC A (English)	200015	53099
Total word count - document A		53593
Total word count - document B		0
Total word count - documents A + B		53593

...ABSTRACT point digital signal processor (DSP) with variable instruction length, offering both high code density and easy programming. Architecture and instruction set are optimized for low **power consumption** and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks. The processor includes an instruction buffer unit...

...modes, such as circular buffer addressing, further support execution of DSP algorithms. The processor includes a multistage execution pipeline with pipeline protection features. Various functional **modules** can be **separately powered down to conserve power**. The processor includes emulation and code debugging facilities with support for **cache** analysis.

...SPECIFICATION point digital signal processor (DSP) with variable instruction length, offering both high code density and easy programming. Architecture and instruction set are optimized for low **power consumption** and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks. The processor includes an instruction buffer unit...

...modes, such as circular buffer addressing, further support execution of DSP algorithms. The processor includes a multistage execution pipeline with pipeline protection features. Various functional **modules** can be **separately powered down to conserve power**. The processor includes emulation and code debugging facilities with support for **cache** analysis.

BRIEF DESCRIPTION OF THE DRAWINGS

Particular embodiments in accordance with the invention will now be described, by way of example only, and with reference...execution pipeline connected to the program flow control unit, the execution pipeline having pipeline protection features. An emulation and code debugging facility with support for **cache** analysis, **cache** benchmarking, and **cache** coherence management is connected to the program flow control unit, to the address/data **unit**, and to the data computation **unit**. Various functional **modules** can be **separately powered down to conserve power**.

In another form of the invention, the processor has a **cache** connected between the instruction memory and the memory interface unit, with a memory management interface connected to the memory interface unit, the memory management unit...

...CLAIMS execution pipeline connected to the program flow control unit; the execution pipeline having pipeline protection features; an emulation and code debugging facility with support for **cache** analysis, **cache** benchmarking, and **cache** coherence management connected to the program flow control unit, to the address/data **unit**, and to the data computation **unit**; and wherein various functional **modules** can be **separately powered down to conserve power**.

2. The digital system of Claim 1, further comprising:

- a **cache** connected between the instruction memory and the memory interface unit; and
- a memory management interface connected to the memory interface unit, the memory management unit...

01082694

Multi-way cache apparatus and method

Mehrweg-Cachespeichervorrichtung und Verfahren

Dispositif d'antememoire a voies multiples et procede

PATENT ASSIGNEE:

MOTOROLA, INC., (205770), 1303 East Algonquin Road, Schaumburg, IL 60196,

(US), (Applicant designated States: all)

INVENTOR:

Moyer, William C., 1005 Pier Branch Road, Dripping Springs, TX 78620,

(US)

LEGAL REPRESENTATIVE:

Gibson, Sarah Jane et al (73531), Motorola European Intellectual Property

Operations Midpoint Alencon Link, Basingstoke, Hampshire RG21 7PL, (GB)

PATENT (CC, No, Kind, Date): EP 952524 A1 991027 (Basic)

APPLICATION (CC, No, Date): EP 99107273 990414;

PRIORITY (CC, No, Date): US 62571 980420

DESIGNATED STATES: DE; FR; GB; IT; NL

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06F-012/08

ABSTRACT WORD COUNT: 151

NOTE:

Figure number on first page: 5

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9943	719
SPEC A	(English)	9943	2623
Total word count - document A			3342
Total word count - document B			0
Total word count - documents A + B			3342

...SPECIFICATION access data having a data class type. Similarly, for each cache way, a particular cache control bit within field 106 will determine whether that particular **cache** way can be used to access data having an instruction class type. While only the class types of data and instruction type have been disclosed...

...for each way of the multi-way cache, at step 206. Selected ways of the cache are enabled based on the enable signals while non- **selected ways** remain **disabled** .. step 208.

When accessing the cache, if there is a cache hit, step 210, the cache access continues with only the selected cache ways participating...

...with the data block from external memory corresponding to the appropriate access operation. The access operation is then completed, step 216.

The above multi-way **cache** apparatus and method has many benefits. For example, in certain processing applications, **cache** efficiency may be increased by providing higher allocation to certain data class types that are more often used by such application. For example, in certain applications, a higher percentage of instruction type data is accessed for processing and would therefore benefit from a higher **cached** usage. By allowing selective allocation of **cache** resources on a multi way basis, such preferred **cache** allocation can be allotted. In addition, since individual **cache** ways may be de-selected for particular data class types, power savings result from non- **use** of associated **power consuming** circuitry for the non-selected cache ways. Such **conservation** of **power** dissipation may be especially useful in many low **power usage** applications, such as in low power handled devices.

Thus, there has been described herein an embodiment including at least one preferred embodiment of an improved...

9/3,K/3 (Item 3 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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01034865

Improvements in or relating to computer memories
Verbesserungen an oder bei Rechnerspeichern
Améliorations relatives pour mémoires de calculateur

PATENT ASSIGNEE:

TEXAS INSTRUMENTS INCORPORATED, (279074), P.O. Box 655474, 13500 Central
Expressway, Dallas, TX 75265, (US), (Applicant designated States: all)

INVENTOR:

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Tran, Hiep Van, 5017 Willow Lane, Dallas, TX 75244, (US)

LEGAL REPRESENTATIVE:

Holt, Michael (50425), Texas Instruments Ltd., PO Box 5069, Northampton,
Northamptonshire NN4 7ZE, (GB)

PATENT (CC, No, Kind, Date): EP 920030 A2 990602 (Basic)
EP 920030 A3 990811

APPLICATION (CC, No, Date): EP 98309665 981125;

PRIORITY (CC, No, Date): US 67293 P 971126

DESIGNATED STATES: DE; FR; GB; IT; NL

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G11C-015/04

ABSTRACT WORD COUNT: 170

NOTE:

Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9922	1089
SPEC A	(English)	9922	7313
Total word count - document A			8402
Total word count - document B			0
Total word count - documents A + B			8402

...SPECIFICATION or other circuitry in controller 21. This programmability can be implemented as either factory or field (user) programmability. This programmability of tag lengths can be used to save power and match times for shorter tags.

Further savings in power usage and match times can be accomplished by disabling the components of tag compare circuit 25 associated with empty cache rows. For example, tag memory 20 might be capable of storing tags for 1K cache rows. However, if the tag memory 20 is not full, sense amps 25a and logic elements 25b - 25e associated with unused rows can be disabled.

As a specific implementation of enabling tag comparisons only for tags that are actually stored, a tag memory can be partitioned into sections. FIGURE 7 illustrates a tag memory 40 partitioned in teachings disclosed herein. Each...

9/3,K/4 (Item 4 from file: 348)

DIALOG(R) File 348:EUROPEAN PATENTS

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00844682

Logical address bus architecture for multiple processor systems
Logische Adressbusarchitektur für Mehrprozessorsysteme
Architecture de bus d'adresse logique pour systèmes multiprocesseurs

PATENT ASSIGNEE:

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Armonk, N.Y. 10504, (US), (Proprietor designated states: all)

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PATENT (CC, No, Kind, Date): EP 780774 A1 970625 (Basic)

APPLICATION (CC, No, Date): EP 96308461 961122;
 PRIORITY (CC, No, Date): US 573683 951218
 DESIGNATED STATES: DE; FR; GB
 INTERNATIONAL PATENT CLASS: G06F-015/16; G06F-013/364
 ABSTRACT WORD COUNT: 214

NOTE:

Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; English
 FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB97	754
CLAIMS B	(English)	200138	520
CLAIMS B	(German)	200138	464
CLAIMS B	(French)	200138	571
SPEC A	(English)	EPAB97	2728
SPEC B	(English)	200138	2785
Total word count - document A			3483
Total word count - document B			4340
Total word count - documents A + B			7823

...SPECIFICATION for processing units with associate cache requires the common connection to address/command bus 2.

Common address/command bus 2 provides the information resource for cache coherence, but does so at the expense of introducing electrical loading and associated clock frequency limiting. Conventional load buffering latches for clock synchronized computer systems...

...the activation of the elected master's drivers to avoid a driver overlap condition.

The logical bus architecture of Fig. 2 also provides resources for selectively disabling ports connecting individual processing units. This capability facilitates the isolation of processing units for fault testing, power conservation, or the like.

The embodiment depicted in Fig. 2 shows a multiplicity of central processing units (CPUs) 13-18 electrically connected through their address/command...

...SPECIFICATION for processing units with associate cache requires the common connection to address/command bus 2.

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The embodiment depicted in Fig. 2 shows a multiplicity of central processing units (CPUs) 13-18 electrically connected through their address/command...

9/3,K/5 (Item 5 from file: 348)

DIALOG(R) File 348:EUROPEAN PATENTS

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00823568

OSCILLATOR INTERFACE FOR USE IN A POWER MANAGEMENT SYSTEM
 OSZILLATOR ZUR VERWENDUNG IN EINER LEISTUNGSSTEUERSYSTEM
 INTERFACE OSCILLATEUR POUR SYSTEME DE GESTION DE PUISSANCE
 PATENT ASSIGNEE:

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PATENT (CC, No, Kind, Date): EP 772911 A1 970514 (Basic)

EP 772911 B1 030903

WO 96037960 961128

APPLICATION (CC, No, Date): EP 96916586 960523; WO 96US7571 960523

PRIORITY (CC, No, Date): US 451206 950526

DESIGNATED STATES: DE; GB

INTERNATIONAL PATENT CLASS: G06F-001/26

NOTE:

No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200336	253
CLAIMS B	(German)	200336	252
CLAIMS B	(French)	200336	290
SPEC B	(English)	200336	5153
Total word count - document A			0
Total word count - document B			5948
Total word count - documents A + B			5948

...SPECIFICATION NOTE: after being turned back on, it will take approximately 1 msec for the external crystal to stabilize). Second, if an external oscillator is being **used**, **Power** Down mode will disable all the system 32 clocks except for the RTC(underscore)osc. (NOTE: This is much faster upon recovery, as there is...

...2) can be individually disabled. The ECP 44 and the Three-wire Serial Interface 50: 1) Connected to OSC(underscore)CLK/2; 2) can be **individually disabled**. The DMA Controller 36 and Bus Interface Unit 42: 1) Uses cpu(underscore)clk (full speed or divided). The DRAM Controller 38: 1) Must use OSC(underscore)CLK for DRAM refresh cycles; 2

...RTC interface. The Global Peripheral Clock Disable/Enable: 1) Controls DMA Controller, ECP, Three-wire Interface, and UART.

The power management system 30 includes several **power** management modes. **Power saving** features include the following. In Idle Mode the internal clock to the CPU 34 will be disabled. All enabled peripheral blocks will continue to operate...

...will re-enable the internal clock to the CPU 34. It should be noted that when the CPU 34 is in Idle Mode, the instruction **cache** cannot snoop. Normally, the **cache** will snoop the addresses to see if a **cache** address is being updated. If so, it flushes the **cache**. Therefore, the user's can take the appropriate action when the CPU 34 is idled. Also, when the CPU 34 is in Idle Mode, the...

9/3,K/6 (Item 6 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

(c) 2004 European Patent Office. All rts. reserv.

00810754

A CACHE COHERENT MULTIPROCESSING COMPUTER SYSTEM WITH REDUCED POWER OPERATING FEATURES

EIN CACHEKOHARENTES MULTIPROZESSORSYSTEM MIT VERMINDERTEN BETRIEBLEISTUNGSMERKMALEN

SYSTEME INFORMATIQUE MULTIPROCESSEUR A ANTEMEMOIRE COHERENTE CARACTERISEE PAR UNE CONSOMMATION REDUITE D'ELECTRICITE

PATENT ASSIGNEE:

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PATENT (CC, No, Kind, Date): EP 799444 A1 971008 (Basic)

EP 799444 A1 980325

EP 799444 B1 031203

WO 96032671 961017

APPLICATION (CC, No, Date): EP 95944751 951220; WO 95US16601 951220

PRIORITY (CC, No, Date): US 363735 941223

DESIGNATED STATES: FR; GB

INTERNATIONAL PATENT CLASS: G06F-001/32; G06F-012/00; G06F-013/00

ABSTRACT WORD COUNT: 4196

NOTE:

No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200349	284
CLAIMS B	(German)	200349	272
CLAIMS B	(French)	200349	323
SPEC B	(English)	200349	3719
Total word count - document A			0
Total word count - document B			4598
Total word count - documents A + B			4598

...SPECIFICATION to all units of the integrated circuit. When the processor enters a low-power or STANDBY state as a result of the assertion of either the STPCLK# pin or the execution of a HALT instruction, the internal clock signal (ICLK) on line 46 is disabled. It should be understood, however, that disabling line 46 does not alter the continuous functioning of PLL circuit 30. In other words, PLL 30 continues to generate an internal core CLK frequency on line 45 coupled to certain portions of microprocessor 20. The portions of microprocessor 20 which remain operational (i.e., activated by CLK) include PLL 30, the tag comparison arrays of cache units 25 and 26, a portion of interrupt logic unit 29 and bus unit 40. In accordance with the present invention, providing power to the selected portions of microprocessor 20 allows the processor to monitor and respond to external bus traffic for the purpose of maintaining cache coherency in MP systems. That is, bus arbitration and cache coherency mechanisms are intentionally kept active in a reduced power mode of operation.

Referring now to Figure 2, there is shown a state diagram illustrating

...

...of one embodiment of the present invention. In normal operating conditions, state 51, microprocessor 20 is active executing instructions. This represents the processor's full power state in which both the ICLK and CLK signals are coupled to all portions of the IC's internal logic.

The STOP(underscore)GRANT state, represented by block...

...can be entered by asserting the external STPCLK# pin of microprocessor 20. In the STOP(underscore)GRANT state the integrated circuit operates in a reduced power consumption mode wherein most of the internal functional units of the processor are deactivated (i.e., ICLK off). On the other hand, bus unit 40, the...

...56 back to AUTO(underscore)HALT state 50.

Figure 2 also includes state 52 which represents the snooping ability of the processor when operating in a reduced power mode, as would be the case following the assertion of the STPCLK# pin or the execution of a HALT instruction. Even though power...

...control logic, and buses between the data cache and bus interface) other than the tag arrays are awakened only if a write-back cycle is required

. In an alternative embodiment, more aggressive power saving may be achieved by **disabling** the **tag** comparison logic in **certain** situations, e.g., all the **cache** entries are invalid, or to **power down** the **tag** arrays until a snoopable transaction has been detected then provide a slightly increased power state to allow the tags to perform the snoop operation.

Note...

...the many different ways that the present invention may be implemented.

Figure 3 illustrates a timing diagram showing the latency between a STPCLK# request and the STOP(underscore)GRANT bus cycle. Note that for the illustrative **embodiment**, there is a delay of approximately **ten** clocks between the STPCLK# request and the STOP(underscore)GRANT bus cycle. This latency is **dependent** upon the current instruction, the amount of data in the CPU write buffers, and system memory performance.

Data **cache** 26 of processor 20 utilizes the MESI protocol to enforce **cache** consistency. A line in the data cache can be in the Modified, Exclusive, Shared or Invalid state, whereas a line in instruction cache 25 can be either in the Valid...

...was completing the snoop transaction. Note that in Figure 4C, two private arbitration pins coupled between the two processors are utilized to indicate that bus **ownership** has been granted to processor PB)) (or that processor PA)) requests ownership back after completion of the writeback operation).

Finally, in Figure 4D processor PA)) reruns the original write cycle after processor PB has granted the bus back to **processor** PA)). It is important to recognize that **processor** PB)) has remained in a reduced **power consumption** mode of operation throughout the entire snoop and writeback processes represented by Figures 4A - 4D. This is a key feature of the present invention since it provides a considerable advantage in computer systems limited by **power consumption** requirements, but yet having a need for **cache** coherency.

With reference now to Figure 5, there is shown a specialized test register 12 which **includes** bits to allow software to **disable certain** features of microprocessor 20. For example, the AUTO(underscore)HALT feature may be **disabled** to setting bit 6 in register 12 to a "1". In this setting, the execution of a HALT instruction does not disable the internal clock...

9/3,K/7 (Item 7 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00646221

Fully integrated cache architecture.

Vollig integrierte Cache-Speicherarchitektur.

Architecture d'antememoire entierement integree.

PATENT ASSIGNEE:

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LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 624844 A2 941117 (Basic)

EP 624844 A3 941214

APPLICATION (CC, No, Date): EP 94103887 940314;

PRIORITY (CC, No, Date): US 60776 930511

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-012/08;

ABSTRACT WORD COUNT: 134

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text Language Update Word Count

CLAIMS A	(English)	EPABF2	2078
SPEC A	(English)	EPABF2	8555
Total word count	- document A		10633
Total word count	- document B		0
Total word count	- documents A + B		10633

...SPECIFICATION an object of the present invention to provide an integrated cache that stores both data and the associated access information in a manner that reduces **power consumption**.

It is another object of the present invention to provide an integrated cache architecture that provides a true least recently used cache update procedure.

It...

...area on the chip. For instance, the cache can be reduced to a 3-way set-associative or enlarged to a 5-way set associative **cache**. A few more bit lines can be added to provide parity checking. Note that the LRU array once initialized has constant parity, such that parity checking may be added thereto with no additional bit lines.

The foregoing and other objects of the present invention are realized by a **cache** formed on an integrated circuit chip for storing data fetched from a main storage means, comprising a plurality of index lines, each of said index first storage array is to be accessed; and an array controller for **selectively deactivating** at least a **portion** of said first storage array of said **selected** one of said plurality of index **lines** before an access cycle thereto has been completed.

In another aspect of the present invention, the **cache** array comprises a plurality of memory cells; a plurality of supply voltage lines disposed above and coupled to said plurality of memory cells; a plurality...

9/3,K/8 (Item 8 from file: 348)
 ANALOG(R)File 348:EUROPEAN PATENTS
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00165427

Microcomputer memory and method for its operation.

Mikrocomputerspeicher und dessen Betriebsverfahren.

Memoire de micro-ordinateur et son procede de fonctionnement.

PATENT ASSIGNEE:

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PATENT (CC, No, Kind, Date): EP 175080 A2 860326 (Basic)
 EP 175080 A3 880727
 EP 175080 B1 911113

APPLICATION (CC, No, Date): EP 85108699 850712;

PRIORITY (CC, No, Date): US 651562 840918

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-012/08;

ABSTRACT WORD COUNT: 148

LANGUAGE (Publication,Procedural,Application): English; English; English

TEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	814
CLAIMS B	(German)	EPBBF1	817
CLAIMS B	(French)	EPBBF1	960
SPEC B	(English)	EPBBF1	3032
Total word count	- document A		0
Total word count	- document B		5623
Total word count	- documents A + B		5623

...SPECIFICATION handshake protocol with the bus. For each bank, the memory controller maintains two fields, the number of the row which is currently in the d- cache and a valid entry flag for the d- cache as shown in the table below: (see image in original document)

The valid bits for all banks are set to invalid (= 0) after power-on. The DRAMs use the buffer also during the refresh operation, destroying the d- cache contents. Thus, the valid bits are also set to 0 following a refresh operation in a bank.

On being accessed from the bus, the memory...

...is as follows: (see image in original document)

The memory controller 18 determines if the accessed row for that bank is already in the d- cache (a hit). If it is, then the memory controller sends out the column address (position within the d- cache) and activates the column address select (CAS) line for that bank. An active CAS for a bank selects that bank for access. Such a hit access is very fast, on the order of 35 to 40 ns. If the accessed word is not in the d- cache (a miss), then the contents of the d- cache have to be switched. To do that, the row address select (RAS) for that bank is made inactive and made active again with the row number of the new address. This operation, taking only 130 ns., writes back the d- cache contents into the DRAM cell matrix and loads the entire new row into the d- cache . This extremely short time needed to switch the entire d- cache contents is one of the major reasons for the good performance of the operation. The accessed word is read into latch 26 from memory 12...

...With 256 rows, a row in a bank has to be refreshed, on an average, every 16 microseconds. Since a refresh operation destroys the d- cache contents, every 16 microseconds, the d- cache is declared invalid and the first access following refresh will be a miss. Thus, the d- cache maximum life expectancy, due to refresh, is 16 microseconds. With the availability of extended refresh (64 milliseconds) DRAMs, this is improved to 256 microseconds. To...

9/3,K/9 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00952055 **Image available**

IN SITU RECOVERY FROM A RELATIVELY LOW PERMEABILITY FORMATION CONTAINING
HEAVY HYDROCARBONS
RECUPERATION IN SITU DANS UNE FORMATION A PERMEABILITE RELATIVEMENT BASSE
CONTENANT DES HYDROCARBURES

Patent Applicant/Assignee:

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Austin, TX 78767-0398, US,
Patent and Priority Information (Country, Number, Date):
Parent: WO 200286029 A2 20021031 (WO 0286029)
Application: WO 2002US13121 20020424 (PCT/WO US0213121)
Priority Application: US 2001286083 20010424; US 2001340185 20011024
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
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Fulltext Word Count: 417978

Fulltext Availability:
Detailed Description
Detailed Description
... bus (as shown in FIG. 18) or may share CPU bus 6295 with processor
6293.

Furthermore, processor 6291 may be coupled to an optional L2 cache 6298
similar to L2 cache 6297.

57

FIG. 19 illustrates a flow chart of a computer-implemented method for
treating a hydrocarbon formation based on a characteristic of the
formation...

9/3,K/10 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00922144 **Image available**
METHOD AND SYSTEM FOR COMMUNITY DATA CACHING
PROCEDE ET SYSTEME DE COMMUNICATION DE MISE EN ANTEMEMOIRE DE DONNEES DE
COMMUNAUTE

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200256182 A2-A3 20020718 (WO 0256182)

Application: WO 2002US886 20020110 (PCT/WO US0200886)

Priority Application: US 2001759392 20010112; US 2001759406 20010112

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ (utility model) CZ DE (utility model) DE DK (utility model) DK DM DZ

EC EE (utility model) EE ES FI (utility model) FI GB GD GE GH GM HR HU ID

IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ

NO NZ OM PH PL PT RO RU SD SE SG SI SK (utility model) SK SL TJ TM TN TR

TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

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Fulltext Word Count: 23091

Fulltext Availability:

Detailed Description

Detailed Description

... a cable modem and a LAN would be considered as creating "always-on" connection.

The growing availability of "always-on" connections provides the opportunity to **utilize** the processing power and storage capacity of computers connected via "always-on" connections to the Internet or other networks. Many computers with "always-on" connections...

...service.

Each cache module 26 is further operable to generate a cache status message 27. Cache status message 27 comprises an indication of whether a **particular** cache module 26 is active or **inactive**. More specifically, cache status message 27 includes a "cache on" or a "cache off" indication. The " **cache** on" indication indicates that the associated **cache** module 26 has gone from an inactive to an active state and is requesting to join community 15. The " **cache** off" indication indicates that the associated **cache** module 26 is going from an active to an inactive state and is requesting removal from community 15. **Cache** status message 27 may also include an "active" indication. The active indication indicates that the associated **cache** module 26 is currently active, and **caching** content and handling requests for content from browsers 30. The active indication may operate as a heartbeat indicating that the associated **cache** module 26 is alive.

Each **cache** module 26 further comprises a distinct location table 29. Location table 29 comprises one or more indications of the location within community 15 of **cached** content. More specifically, location table 29 indicates which client 12 is responsible for **caching** which content.

In general, table 29 may use any suitable indication for indicating which clients 12 to **cache** content at, such as IP addresses, domain names, portions of URLs or a hash value based on a content request from browser 30.

Cache modules 26 may be further operable to provide increased anonymity while surfing to users of clients 12.

5 More specifically, cache module 26 may remove...

9/3,K/11 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00485834 **Image available**

LOCALIZED PERFORMANCE THROTTLING TO REDUCE IC POWER CONSUMPTION
REGULATION LOCALISEE DU FONCTIONNEMENT POUR REDUIRE LA CONSOMMATION
D'ENERGIE DE CIRCUITS INTEGRES

Patent Applicant/Assignee:

INTEL CORPORATION,

Inventor(s):

MITTAL Millind,

VALENTINE Robert,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9917186 A1 19990408

Application: WO 97US17492 19970929 (PCT/WO US9717492)

Priority Application: WO 97US17492 19970929

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DK DK EE EE ES FI FI GB GE GH HU ID IL IS JP KE KG KP KR KZ LC LK LR LS
LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM
TR TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ
TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM
CA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 10786

Fulltext Availability:

Detailed Description

Detailed Description

... also

reduce performance. Thus, there is a need to reduce the power
consumed by an IC without reducing its performance.

For many complex ICs, the **power** consumed varies widely with
the task that they are performing. If more of the circuit nodes within
the

IC transition from one to zero or...would be useful, for example, in
estimating the
battery life of a portable computing device under normal use.

It is desirable to reduce the power **consumed** by an IC by
reducing or eliminating node transitions in functional units within the
IC that are not being used during a particular sequence of operations.
If an
IC shuts down functional units when they are not being **used**, then
typical **power consumption** can be significantly reduced with little or
no
impact on performance.

4. However, shutting down functional units is likely to have little
impact on worst-case **power consumption**, which often arises when the
IC is performing sequences of operations that utilize many of the
functional units within the IC. Worst-case **power consumption** is
likely to be substantially higher than typical **power consumption**.

5 Often particular functional units or logic blocks within an IC can
be identified that tend to consume a disproportionate share of the IC's
power -- for example, the circuitry in a microprocessor that performs
floating-point arithmetic. The **power consumed** by a microprocessor is
significantly less if it is not called on to perform many floating-point
operations.

The worst-case **power consumption** of a microprocessor might
involve a sequence of floating point operations that operates on data
values chosen to maximize node transitions from one to zero...

...reading or writing main memory.

Additionally, if the microprocessor performs speculative evaluations of upcoming operations based on predicting which way a branch operation will go, **power consumption** would be increased by increasing the percentage of branch operations for which the microprocessor's prediction is accurate. This is because an inaccurate prediction flushes ...mode, i.e. accesses to it are denied. This preferably forces the processor into an idle or wait state if it attempts to reference the **cache** when **cache** unavailable 312 is asserted.

The values in threshold register 306, inactive decrement register 305, and active increment register 304 can be programmable by a variety...

...active increment register 304 and inactive decrement register 305 can be selected to enforce a wide range of maximum duty cycles on the on chip **cache**. Further, the value of threshold register 306 can be programmed to vary the maximum duration of bursts of high **cache** activity. This enables high performance on sequence of operations that require bursts of **cache** accesses -- at least for those bursts of duration 10 within tolerable **power - consumption** limits.

Design Alternatives for Programmability

The invention is flexible in that it encompasses a wide range of design alternatives for programming or setting the contents of the 15 throttling parameters associated with a **particular** functional unit, i.e. of threshold register 306, **inactive** decrement register 305, and active increment register 304. They could be read-only values programmed to the desired value like a read-only memory (ROM...

...one-time-only writing process such as blowing a fusible link for each bit. These design alternatives allow different versions of the IC with different **power consumption** and performance specifications.

Alternatively, programming the throttling-parameter values could be under software control -- either under control of the platform software or basic input/output...

9/3,K/12 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00355446 **Image available**

CONFIGURABLE POWER MANAGEMENT SCHEME PLAN DE GESTION DE PUISSANCE CONFIGURABLE

Patent Applicant/Assignee:

NATIONAL SEMICONDUCTOR CORPORATION,

Inventor(s):

SHAY Michael J,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9637960 A2 19961128

Application: WO 96US7571 19960523 (PCT/WO US9607571)

Priority Application: US 95451206 19950526

Designated States: DE KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Publication Language: English

Fulltext Word Count: 7976

Fulltext Availability:

Detailed Description

Detailed Description

... NOTE: after being turned back on, it will take approximately 1 rnscc for the external crystal to stabilize). Second, if an external oscillator is being **used**, **Power** Down mode will disable all the system 32 clocks except for the RTC-osc. (NOTE: This is much faster upon recovery, as

there is no...

...OSC; 2) can be individually disabled. The ECP 44 and the Three-wire Serial Interface 50: 1) Connected to OSC-CLK/2; 2) can be **individually disabled**. The DMA Controller 36 and Bus Interface Unit 42: 1) Uses cpu-clk (full speed or ...RTC interface.

The Global Peripheral Clock Disable/Enable: 1) Controls DMA Controller, ECP, Three-wire Interface, and UART.

The power management system 30 includes several **power** management modes. **Power saving** features include the following. In Idle Mode the internal clock to the CPU 34 will be disabled. All enabled peripheral blocks will continue to operate...

...will re-enable the internal clock to the CPU 34. It should be noted that when the CPU 34 is in Idle Mode, the instruction **cache** cannot snoop. Normally, the **cache** will snoop the addresses to see if a **cache** address is being updated. If so, it flushes the **cache**. Therefore, the user's can take the appropriate action when the CPU 34 is idled. Also, when the CPU 34 is in Idle Mode, the...

9/3,K/13 (Item 5 from file: 349)
FILE: File 349: PCT FULLTEXT
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0350153

A CACHE COHERENT MULTIPROCESSING COMPUTER SYSTEM WITH REDUCED POWER OPERATING FEATURES

SYSTEME INFORMATIQUE MULTIPROCESSEUR A ANTEMEMOIRE COHERENTE CARACTERISEE PAR UNE CONSOMMATION REDUITE D'ELECTRICITE

Patent Applicant/Assignee:

INTEL CORPORATION,

Inventor(s):

CARMEAN Douglas M,

CRAWFORD John,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9632671 A1 19961017

Application: WO 95US16601 19951220 (PCT/WO US9516601)

Priority Application: US 94363735 19941223

Designated States: AL AM AT AU BB BG BR BY CA CH CN CZ CZ DE DE DK DK EE
EE ES FI FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN
MW MX NO NZ PL PT RO RU SD SE SG SI SK SK TJ TM TT UA UG UZ VN KE LS MW
SD SZ UG AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI
CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 4315

Fulltext Availability:

Detailed Description

Detailed Description

... the snooping

ability of the processor when operating in a reduced power mode, as WO 96/32671 PCTfUS95116601 I 0

processor snoops -- by keeping the **cache** units tag comparison logic enabled by CLK This is illustrated in Figure 1, wherein the CLK signal on line 45 is coupled to the tag comparison logic of **caches** 25 and 26.

On the other hand, the ICLK signal is disabled to the data array portions of the **caches** to minimize power consumption. When a snoop occurs, the MESI (i.e., Modified, Exclusive, Shared, Invalid) **cache** protocol bits

are updated when the need arises. Portions of the processor (e.g., at least the data **cache**, associated **cache** control logic, and buses between the data **cache** and bus interface) other than the tag arrays are awakened only if a write-back cycle is required. In an alternative embodiment, more aggressive power saving may be achieved by

disabling the tag comparison logic in certain situations, e.g., all the cache entries are invalid, or to power down the tag arrays until a snooperable transaction has been detected then provide a slightly increased power state to allow the tags to perform the snooper operation.

Note...

...GRANT bus cycle. This latency is dependent upon the current instruction, the amount of data in the CPU write buffers, and system memory performance.

Data cache 26 of processor 20 utilizes the MESI protocol to enforce cache consistency. A line in the data cache can be in the Modified, Exclusive, Shared or Invalid state, whereas a line in instruction cache 25 can be either in the Valid or Invalid...

9/3,K/14 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00242159 **Image available**
HARDWARE EMULATION ACCELERATOR AND METHOD
PROCEDE ET ACCELERATEUR CONCERNANT L'EMULATION DE MATERIELS INFORMATIQUES
Patent Applicant/Assignee:
SEIKO EPSON CORPORATION,
Inventor(s):
LIN Chong Ming,
NGUYEN Le Trong,
HO Wai-Yan,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9316433 A1 19930819
Application: WO 93JP149 19930205 (PCT/WO JP9300149)
Priority Application: US 92831272 19920207
Designated States: JP AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 6697

Fulltext Availability:
Detailed Description

Detailed Description

... working
CPU 706 and clock generator 708. The second N-bit microprocessor chip labeled 710 includes a working FPU 712 and TLB 714. A first cache memory unit chip 716 includes a working cache controller 718 and a second cache memory unit chip 720 includes a working cache RAM 722.

An external bus is used to interconnect the chips. Because the paths between the functional modules are longer on hardware emulation accelerator 700...added to the system so that additional control or functionality can be added. Software block 724 thus provides a means of flexibly changing control of modules or blocks or added functionality to the hardware emulation accelerator.

By employing "selective power down" of the functional modules not used for the hardware emulator accelerator, further power saving and prolonging of chip life time can be achieved. Since static CMOS circuits use negligible power when not switching, selective power down can be implemented by not providing clock signals or input signals to the unused

15/3,K/29 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00730902 **Image available**

I/O CACHE WITH USER CONFIGURABLE PRELOAD

ANTEMEMOIRE D'ENTREE/SORTIE A PRECHARGEMENT CONFIGURABLE PAR UN UTILISATEUR

Patent Applicant/Assignee:

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(Residence), US (Nationality), (For all designated states except: US)

Patent Applicant/Inventor:

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Legal Representative:

MILLIKEN Darren J, Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor,
12400 Wilshire Boulevard, Los Angeles, CA 90025, US

Patent and Priority Information (Country, Number, Date):

Patent: WO 200043889 A1 20000727 (WO 0043889)

Application: WO 2000US2156 20000125 (PCT/WO US0002156)

Priority Application: US 99237990 19990126

Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK

DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR

LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ

TM TR TT TZ UA UG US UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 13742

Fulltext Availability:

Detailed Description

Detailed Description

... In many modern computer systems, a reduced level of system power, called "trickle power," is available so long as the computer system is connected to line power. In such systems, trickle power can be used to power the user cache even when the computer system is turned off. When system power is lost entirely, the power source selector detects the power loss and switches to the battery 65 to maintain power to the...

...In the reduced power state, DRAM refresh operations are continued either under control of the DRAM controller 63 or by logic on board the DRAM components themselves. Other logic elements within the user-cache 25, including the bus interface circuitry 61 and portions of the DRAM controller that operate on access requests from the bus interface circuitry are shut down to save power. Unused rows of the DRAM array may be shut down to save power.

In one embodiment, the expansion bus 18 of Fig. 1 is a peripheral component interconnect (PCI) bus and the bus interface circuitry 61 of the user cache 25 is a PCI bus interface for sending and receiving data, address and control signals on the PCI bus. Herein, PCI bus refers to a...

15/3,K/30 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00730867 **Image available**

PRELOADING DATA IN A CACHE MEMORY ACCORDING TO USER-SPECIFIED PRELOAD CRITERIA

• PRECHARGEMENT DE DONNEES DANS UN CACHE EN FONCTION DE CRITERES DE
PRECHARGEMENT SPECIFIES PAR L'UTILISATEUR

Patent Applicant/Assignee:

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(Residence), US (Nationality), (For all designated states except: US)

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Legal Representative:

MILLIKEN Darren J (et al) (agent), Blakely, Sokoloff, Taylor & Zafman
LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200043854 A2-A3 20000727 (WO 0043854)

Application: WO 2000US1916 20000125 (PCT/WO US0001916)

Priority Application: US 99238656 19990126

Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK
DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ
TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OAPI utility model) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 11064

Fulltext Availability:

Detailed Description

Detailed Description

... man modem computer systems, a reduced level of system power, called
... y
"trickle power," is available so long as the computer system is connected
to line power. In such systems, trickle power can be used to
power the user cache even when the computer system is turned off .
When system power is lost entirely, the power source selector detects the
power loss and switches to the battery 65 to maintain power to the...
...In the reduced power state, DRAM refresh operations are continued either
under control of the DRAM controller 63 or by logic on board the DRAM
components themselves. Other logic elements within the user- cache
25, including the bus interface circuitry 61 and portions of the DRAM
controller that operate on access requests from the bus interface
circuitry are shut down to save power . Unused rows of the DRAM
array may be shut down to save power .

In one embodiment, the expansion bus 18 of Fig. 1 is a peripheral
component interconnect (PCI) bus and the bus interface circuitry 61 of
the user cache 25 is a PCI bus interface for sending and receiving
data, address and control signals on the PCI bus. Herein, PCI bus refers
to a...

15/3,K/31 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00442644 **Image available**

METHOD AND APPARATUS FOR TOLERATING POWER OUTAGES OF VARIABLE DURATION IN A
MULTI-PROCESSOR SYSTEM

PROCEDE ET DISPOSITIF PERMETTANT DE SUPPORTER DES COUPURES DE COURANT DE
DUREE VARIABLE DANS UN SYSTEME MULTIPROCESSEUR

Patent Applicant/Assignee:

TANDEM COMPUTERS INCORPORATED,

Inventor(s):

JARDINE Robert L,

REEVES Larry D,
BASAVAIHA Murali,
EASOP Garry,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9833108 A1 19980730

Application: WO 98US1530 19980127 (PCT/WO US9801530)

Priority Application: US 97789260 19970128

Designated States: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Publication Language: English

Fulltext Word Count: 13968

Fulltext Availability:

Detailed Description

Detailed Description

... low-power instruction, the hardware shuts down power to all disks and tapes in its processor subsystem (and performs other shut down operations such as **powering down** all unnecessary **components**).

In one embodiment, the processor #

240 goes into a

reset state, minimizing its **power consumption** . In another, the processor #-240 continues to execute, perhaps using **cache** memory only, In some implementations, by not accessing main memory, the processors # 240 **consumes less power** . Slowing down the clock to the processor #.240 also results in lower **power consumption** . (Some laptop systems slow down their clocks at certain times to **conserve battery power** ,)

The processor subsystem #

210 may also shut down

cooling fans.

SUBSTITUTE SHEET (RULE 26)

The low-level reset routine never returns. Instead, if the outage...

15/3,K/32 (Item 9 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00396564 **Image available**

METHOD & APPARATUS FOR CONTROLLING POWER CONSUMPTION IN A MICROPROCESSOR
PROCEDE ET DISPOSITIF DE REGULATION DE LA PUISSANCE ABSORBEE DANS UN
MICROPROCESSEUR

Patent Applicant/Assignee:

INTEL CORPORATION,

MATES John William Benson,

Inventor(s):

MATES John William Benson,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9737307 A1 19971009

Application: WO 97US4375 19970319 (PCT/WO US9704375)

Priority Application: US 96623978 19960329

Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE

DK DK EE EE ES FI FI GB GE GH HU IL IS JP KE KG KP KR KZ LK LR LS LT LU

LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK TJ TM TR TT UA

UG US UZ VN YU GH KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH

DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR

NE SN TD TG

Publication Language: English

Fulltext Word Count: 4559

Fulltext Availability:

Detailed Description

Detailed Description

... unit 345 executes the P@tOps by

enabling or disabling clock signals that are coupled to other functional units throughout the microprocessor. These other functional units may include but are not limited to the FEU, IEU, MIU, and AGU. The power unit 345 may also be implemented to control clock signals which are coupled to registers, queues, caches, etc., thereby allowing the Power Unit to control power consumption in any unused or unneeded functional units. By disabling clock signals, the power consumed in the disabled functional units is dramatically reduced.

As shown in Fig. 3, the IFU 320 is coupled to the ID 332. In the present embodiment, the ID 332 provides...

15/3,K/33 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00223839 **Image available**
SUSPEND/RESUME CAPABILITY FOR A PROTECTED MODE MICROPROCESSOR AND HARD
DISK, AND IDLE MODE IMPLEMENTATION
FONCTION ARRET/REPRISE POUR MICROPROCESSEUR ET DISQUE DUR A MODE PROTEGE,
ET APPLICATIONS EN MODE INACTIF

Patent Applicant/Assignee:

ZENITH DATA SYSTEMS CORPORATION,

Inventor(s):

FOSTER Mark J,
FAKHRUDDIN Saifudden T,
WALKER James L,
MENDELOW Matthew B,
SUN Jiming,
BRAHMAN Rodman S,
KRAU Michael P,
WILLOUGHBY Brian D,
MADDIX Michael D,
BELT Steven L,
HOVEY Scott A,
RUTHENBECK Mark A,
MART Gregory Allen,
VANDERHEYDEN Randy J,
GRABON Robert J,
PANDYA Chandrakant H,
TERRY-GRAY Neysa K,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9221081 A1 19921126

Application: WO 92US4169 19920515 (PCT/WO US9204169)

Priority Application: US 9139 19910517; US 9126 19910517; US 91342
19910830; US 9248 19920403; US 92787 19920403

Designated States: AT BE CA CH DE DK ES FR GB GR IT JP LU MC NL SE

Publication Language: English

Fulltext Word Count: 40128

Fulltext Availability:

Detailed Description

Detailed Description

... the maximum clock speed, and thus the slow speed clocks will not be implemented until the saved state information is restored to the processor at block 3112 in Figure 33, or in other words when the application program is resumed, Finally, still in block 3122, the processor 3011 disables the cache memory 3013, In some systems, disabling of the cache memory may cause the system to use more power than when the cache is enabled, in which case disabling of the cache can be omitted, However, in systems where disabling the cache memory reduces power consumption, it is implemented at this point.

File 8: Ei Compendex(R) 1970-2004/Feb W5
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 (c) 2004 INIST/CNRS
 File 434: SciSearch(R) Cited Ref Sci 1974-1989/Dec
 (c) 1998 Inst for Sci Info
 File 34: SciSearch(R) Cited Ref Sci 1990-2004/Feb W5
 (c) 2004 Inst for Sci Info
 File 99: Wilson Appl. Sci & Tech Abs 1983-2004/Feb
 (c) 2004 The HW Wilson Co.
 File 583: Gale Group Globalbase(TM) 1986-2002/Dec 13
 (c) 2002 The Gale Group
 File 266: FEDRIP 2004/Jan
 Comp & dist by NTIS, Intl Copyright All Rights Res
 File 95: TEME-Technology & Management 1989-2004/Feb W3
 (c) 2004 FIZ TECHNIK

Set	Items	Description
S1	43255	CACHE? ? OR CACHING
S2	389495	(POWER??? OR SHUT????) (3W)DOWN OR POWERDOWN OR SHUTDOWN OR SHUTTINGDOWN OR DISABL??? OR DEACTIVAT? OR DE()ACTIVAT? OR INACTIVE OR INACTIVAT? OR (TURN??? OR SWITCH??? OR FLIP???? OR -TOGGL???) (3W)OFF OR INOPERAT? OR DISENGAG?
S3	7998642	INDIVIDUAL? OR INDEPENDENT? OR SEPARATE OR SEPARATELY OR PARTICULAR OR SELECTED OR SELECT OR SELECTIV? OR SPECIFIC OR CERTAIN
S4	2150	S2(7N)S3(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SEGMENT? ? OR CONSTITUENT? ?)
S5	7328272	POWER??? OR POWERUP OR ENABL??? OR ACTIVAT? OR (TURN??? OR SWITCH??? OR FLIP???? OR TOGGL???) (3W)ON OR ENGAG??? OR ELECTRICITY OR CURRENT
S6	49584	S3(7N)S5(7N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SUBCOMPONENT? ? OR CONSTITUENT? ?)
S7	189839	(POWER OR ELECTRICITY) (3N) (CONSUMPTION OR CONSUMED OR CONSUME OR CONSUMES OR CONSUMING OR USE OR USED OR USAGE OR EXPENDITURE? ? OR SAV??? OR CONSERV? OR UTILIZ? OR UTILIS? OR PRESERV? OR SPENT OR SPENDING)
S8	17	S1 AND S4
S9	66	S1 AND S6
S10	23	S9 AND S7
S11	39	S8 OR S10
S12	22	RD (unique items)
S13	13	S12 NOT PY=2001:2004
S14	81	S1(15N)S2(15N) (UNIT? ? OR SECTION? ? OR PART? ? OR MODULE? ? OR ELEMENT? ? OR WAYS OR BANK? ? OR FIELD? ? OR TAG? ? OR VICTIM? ? OR VAU OR LINE? ? OR BLOCK? ? OR PIECE? ? OR PORTION? ? OR COMPONENT? ? OR SEGMENT? ? OR CONSTITUENT? ?)
S15	16	S7 AND S14
S16	10	RD (unique items)
S17	3	S16 NOT PY=2001:2004
S18	16	S15 OR S17
S19	276	AU=(MAIYURAN, S? OR MAIYURAN S? OR MOULTON, L? OR MOULTON -

S20

L?)
0 S1 AND S19

18/5/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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06738115 E.I. No: EIP04098039962

Title: A Compiler Approach for Reducing Data Cache Energy

Author: Zhang, W.; Karakoy, M.; Kandemir, M.; Chen, G.

Corporate Source: CSE Department Penn State Univ., University Park, PA 16802, United States

Conference Title: 2003 International Conference on Supercomputing

Conference Location: San Francisco, CA, United States Conference Date: 20030623-20030626

Sponsor: ACM/SIGARCH; Intel Corporation; Florida State University

E.I. Conference No.: 62275

Source: Proceedings of the International Conference on Supercomputing 2003. p 76-85

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Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)

Journal Announcement: 0403W2

Abstract: Silicon technology advances have made it possible to pack millions of transistors - switching at high clock speeds - on a single chip. While these advances bring unprecedented performance to electronic products, they pose difficult **power /energy consumption** problems. For example, large number of transistors in dense on-chip cache memories **consume** significant static (leakage) **power** even if the cache is not used by the current computation. While previous compiler research studied code and data restructuring for improving data cache performance, to our knowledge, there is no compiler-based study that targets data cache leakage **power consumption**. In this paper, we present code restructuring techniques for array-based and pointer-intensive applications for reducing data **cache** energy consumption. The idea is to let the compiler to analyze the code and insert instructions that **turn off cache lines** that keep variables not used by the current computation. This **turning off** does not destroy contents of a **cache line**, and waking up the **cache line** incurs very little overhead. Due to data locality, we find that at a given time only a small **portion** of the data **cache** needs to be active; the remaining **part** can be placed into a leakage-saving mode (state); i.e., they can be **turned off**. Our preliminary results indicate that the proposed strategy reduces the **cache** energy consumption significantly. We also show that several compiler optimizations increase the effectiveness of our strategy. 41 Refs.

Descriptors: *Program compilers; Cache memory; Microprocessor chips; Energy utilization; Transistors; Data structures; Data storage equipment; Computer architecture; Algorithms

Identifiers: Compiler analysis; Code restructuring; Energy optimization; Data caches

Classification Codes:

723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 525.3 (Energy Utilization); 714.2 (Semiconductor Devices & Integrated Circuits); 723.2 (Data Processing); 723.3 (Database Systems)

723 (Computer Software, Data Handling & Applications); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements); 525 (Energy Management); 714 (Electronic Components & Tubes); 921 (Applied Mathematics)

72 (COMPUTERS & DATA PROCESSING); 52 (FUEL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS)

18/5/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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06086699 E.I. No: EIP02287009149

Title: Drowsy caches: Simple techniques for reducing leakage power

Author: Flautner, Krisztian; Kim, Nam Sung; Martin, Steve; Blaauw, David; Mudge, Trevor

Corporate Source: ARM Ltd, Cambridge, CB1 9NJ, United Kingdom
Conference Title: 29th Annual International Symposium on Computer Architecture
Conference Location: Anchorage, AK, United States Conference Date: 20020525-20020529
Sponsor: IEEE
E.I. Conference No.: 59253
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Publication Year: 2002
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Abstract: On-chip caches represent a sizable fraction of the total **power consumption** of microprocessors. Although large caches can significantly improve performance, they have the potential to increase **power consumption**. As feature sizes shrink, the dominant component of this power loss will be leakage. However, during a fixed period of time the activity in a cache is only centered on a small subset of the lines. This behavior can be exploited to cut the leakage power of large caches by putting the cold cache lines into a state **preserving**, low-**power** drowsy mode. Moving lines into and out of drowsy state incurs a slight performance loss. In this paper we investigate policies and circuit techniques for implementing drowsy caches. We show that with simple architectural techniques, about 80%-90% of the cache lines can be maintained in a drowsy state without affecting performance by more than 1%. According to our projections, in a 0.07 um CMOS process, drowsy caches will be able to reduce the total energy (static and dynamic) consumed in the **caches** by 50%-75%. We also argue that the use of drowsy **caches** can simplify the design and control of low-leakage **caches**, and avoid the need to completely **turn off** selected **cache lines** and lose their state.
12 Refs.

Descriptors: *Cache memory; Microprocessor chips; CMOS integrated circuits; Leakage currents; Adaptive algorithms

Identifiers: Leakage power

Classification Codes:

722.1 (Data Storage, Equipment & Techniques); 714.2 (Semiconductor Devices & Integrated Circuits); 701.1 (Electricity, Basic Concepts & Phenomena)

722 (Computer Hardware); 714 (Electronic Components & Tubes); 701 (Electricity & Magnetism)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 70 (ELECTRICAL ENGINEERING, GENERAL)

18/5/3 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online

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ACHIEVING HIGH PERFORMANCE AND ENERGY EFFICIENCY IN SUPERPIPELINED PROCESSORS (PARALLELISM)

Author: SU, CHING-LONG JIM

Degree: PH.D.

Year: 1995

Corporate Source/Institution: UNIVERSITY OF SOUTHERN CALIFORNIA (0208)

Adviser: ALVIN M. DESPAIN

Source: VOLUME 57/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 1336. 340 PAGES

Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL ; COMPUTER SCIENCE

Descriptor Codes: 0544; 0984

One approach to exploring instruction-level parallelism is superpipelining which uses deep pipelines to achieve high clock rates. Pipeline hazards, memory latency, and **power consumption** are three vital factors that limit the benefits of superpipelining. This dissertation presents several novel approaches to achieve high-performance and

energy-efficient superpipelined microprocessors. These approaches focus mainly on reducing pipeline stalls, memory latency, and energy consumption of unnecessary bit switches.

To reduce the number of pipeline stalls, an optimizing instruction scheduler, named Super-reorderer, was built in which in-block scheduling and cross-block scheduling are applied to minimize the number of data and structural hazards. A novel branch scheme is proposed, called branch with masked squashing, to minimize the number of control hazards. The basic idea of branch with masked squashing is to fill delay slots with safe instructions which may come before or after the branch. For the remaining unfilled delay slots, instructions from the predicted target path are used to fill the delay slots. In the case of misprediction, only unsafe instructions are annulled. The safe instructions in branch delay slots are always executed.

To reduce memory latency, unconventional cache mapping functions, hardware-controlled instruction prefetching, and software-controlled data prefetching techniques are investigated. Two novel unconventional cache mapping functions: bit-flipping and segmented bit-selection are proposed and evaluated. A direct-mapped cache with these unconventional cache mapping functions can achieve high hit rates, while maintaining a hit time as fast as a direct-mapped cache with traditional mapping. A novel technique for software-controlled data prefetching is proposed in which the starting data in a data region of a working set is prefetched by software and the subsequent data in the data region is prefetched by hardware. One of the limitations of the software-controlled data prefetching techniques is the execution overhead caused by prefetch instructions. A novel instruction set is proposed in which non-memory-access operations are combined with an optional prefetch operation to effectively eliminate the execution overhead caused by a prefetch instruction. A novel hardware-controlled instruction prefetching technique, called branch correlation-based cache prefetching (BCCP), is proposed. The BCCP, which takes advantage of high branch prediction accuracies of correlation-based cache prediction and aggressive cache line look ahead prefetching, is able to effectively hide long instruction cache latency.

To reduce energy consumption in a modern instruction set processor, several novel hardware and software techniques are investigated. A software technique, called Cold Scheduling, is proposed to reduce energy consumption in the control path. The basic idea is to apply compilation techniques to reorder instruction sequences such that the amount of bit switching on the control path is minimal during program execution. Dynamic power management, which automatically shuts down power consumption in unused functional units during program execution, is investigated to reduce energy consumption in the data path. Two novel cache design techniques are proposed, namely Gray code addressing and cache partitioning, to reduce energy consumption in the caches. The idea of the Gray code addressing is to minimize the bit switches on address buses and I/O pads which usually consume a significant amount of energy in the caches. The idea of cache partitioning is to minimize average energy consumption in each cache access by vertically or horizontally partitioning cache memory cell arrays. (Abstract shortened by UMI.)

18/5/4 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

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7748969 INSPEC Abstract Number: B2003-11-1265F-021, C2003-11-5130-015

Title: Dead-block elimination in cache: a mechanism to reduce I-cache power consumption in high performance microprocessors

Author(s): Kabadi, M.G.; Kannan, N.; Chidambaram, P.; Narayanan, S.; Subramanian, M.; Parthasarathi, R.

Author Affiliation: Sch. of Comput. Sci. & Eng., Anna Univ., India

Conference Title: High Performance Computing - HiPC 2002. 9th International Conference. Proceedings (Lecture Notes in Computer Science Vol.2552) p.79-88

Editor(s): Sahni, S.; Prasanna, V.K.; Shukla, U.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 2002 **Country of Publication:** Germany **xxi+735 pp.**

ISBN: 3 540 00303 7 Material Identity Number: XX-2002-04055

Conference Title: High Performance Computing HiPC 2002. 9th International Conference. Proceedings

Conference Date: 18-21 Dec. 2002 Conference Location: Bangalore, India

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Both power and performance are important design parameters of the present day processors. We explore an integrated software and circuit level technique to reduce leakage power in L1 instruction caches of high performance microprocessors, by eliminating basic blocks from the cache, as soon as they are dead. The effect of this dead block elimination in cache on both the **power consumption** of the I-cache and the performance of the processor is studied. Identification of basic blocks is done by the compiler from the control flow graph of the program. This information is conveyed to the processor, by annotating the first instruction of selected basic blocks. During execution, the blocks that are not needed further are traced and invalidated and the lines occupied by them are **turned off**. This mechanism yields an average of about 5% to 16% reduction, in the energy consumed for different sizes of I- **cache**, for a set of the SPEC CPU 2000 benchmarks, without any performance degradation. (18 Refs)

Subfile: B C

Descriptors: cache storage; data flow graphs; integrated software; microprocessor chips; **power consumption**; program compilers; program control structures

Identifiers: dead block elimination; I-cache **power consumption**; high performance microprocessor; design parameter; integrated software; L1 instruction cache; control flow graph; SPEC CPU 2000 benchmark; performance degradation

Class Codes: B1265F (Microprocessors and microcomputers); C5130 (Microprocessor chips); C6120 (File organisation); C1160 (Combinatorial mathematics); C6150C (Compilers, interpreters and other processors)

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18/5/5 (Item 2 from file: 2)

DIALOG(R) File 2:INSPEC

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7336315 INSPEC Abstract Number: B2002-09-1265D-022, C2002-09-5320G-010

Title: Drowsy caches: simple techniques for reducing leakage power

Author(s): Flautner, K.; Nam Sung Kim; Martin, S.; Blaauw, D.; Mudge, T.

Author Affiliation: ARM Ltd., Cambridge, UK

Conference Title: Proceedings 29th Annual International Symposium on Computer Architecture p.148-57

Publisher: IEEE Comput. Soc, Piscataway, NJ, USA

Publication Date: 2002 **Country of Publication:** USA xv+332 pp.

ISBN: 0 7695 1605 X **Material Identity Number:** XX-2002-01719

U.S. Copyright Clearance Center Code: 1063-6897/02/\$17.00

Conference Title: Proceedings of 29th Annual International Symposium on Computer Architecture

Conference Sponsor: IEEE Comput. Soc.; ACM

Conference Date: 25-29 May 2002 **Conference Location:** Anchorage, AK, USA

Language: English **Document Type:** Conference Paper (PA)

Treatment: Practical (P)

Abstract: On-chip caches represent a sizable fraction of the total **power consumption** of microprocessors. Although large caches can significantly improve performance, they have the potential to increase **power consumption**. As feature sizes shrink the dominant component of this power loss will be leakage. However, during a fixed period of time the activity in a cache is only centered on a small subset of the lines. This behavior can be exploited to cut the leakage power of large caches by putting the cold cache lines into a state **preserving**, low- **power** drowsy mode. Moving lines into and out of drowsy state incurs a slight performance loss. In this paper we investigate policies and circuit techniques for implementing drowsy caches. We show that with simple architectural techniques, about 80%-90% of the cache lines can be maintained in a drowsy state without affecting performance by more than 1%. According to our projections, in a

0.07 um CMOS process, drowsy caches will be able to reduce the total energy (static and dynamic) consumed in the caches by 50%-75%. We also argue that the use of drowsy caches can simplify the design and control of low-leakage caches, and avoid the need to completely turn off selected cache lines and lose their state. (12 Refs)

Subfile: B C

Descriptors: cache storage; CMOS memory circuits; memory architecture; power consumption; total energy

Identifiers: drowsy caches; leakage power reduction; power consumption; cold cache lines; leakage energy; cache memory; ABB-MTCMOS; CMOS circuits

Class Codes: B1265D (Memory circuits); B2570D (CMOS integrated circuits); C5320G (Semiconductor storage); C5310 (Storage system design)

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18/5/6 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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7226358 INSPEC Abstract Number: B2002-05-2570D-011, C2002-05-5320G-009

Title: Cache-line decay: a mechanism to reduce cache leakage power

Author(s): Kaxiras, S.; Zhigang Hu; Narlikar, G.; McLellan, R.

Conference Title: Power-Aware Computer Systems. First International Workshop, PACS 2000. Revised Papers (Lecture Notes in Computer Science) p.82-96

Editor(s): Falsafi, B.; Vijaykumar, T.N.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 2001 Country of Publication: Germany x+151 pp.

ISBN: 3 540 42329 X Material Identity Number: XX-2001-02460

Conference Title: Power-Aware Computer Systems. First International Workshop, PACS 2000. Revised Papers

Conference Date: 12 Nov. 2000 Conference Location: Cambridge, MA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Reducing the supply voltage to reduce dynamic power consumption in CMOS devices, inadvertently will lead to an exponential increase in leakage power dissipation. We explore an architectural idea to reduce leakage power in data caches. Previous work (Wood et al., 1991) has shown that cache frames are "dead" for a significant fraction of time. We are exploiting this observation to turn off cache lines that are not likely to be accessed any more. Our method is simple: if a cache - line is not accessed within a fixed interval (called decay interval) we turn off its supply voltage using a gated V/sub dd/ technique introduced previously (Powell et al., 2000). We study the effect of cache - line decay on both power consumption and performance. We find that it is possible with cache- line decay to build larger caches that dissipate less leakage power than smaller caches while yielding equal or better performance (fewer misses). In addition, because our method can dynamically trade performance for leakage power it can be adjusted according to the requirements of the application and/or the environment. (11 Refs)

Subfile: B C

Descriptors: cache storage; CMOS memory circuits; low-power electronics

Identifiers: cache-line decay; low power electronics; cache leakage power; supply voltage; dynamic power consumption; CMOS devices; leakage power dissipation; data caches; cache frames; decay interval; gated V/sub dd/ technique

Class Codes: B2570D (CMOS integrated circuits); B1265D (Memory circuits); C5320G (Semiconductor storage)

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18/5/7 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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05672753 JICST ACCESSION NUMBER: 04A0047955 FILE SEGMENT: JICST-E

Way-variable Caches for Static Power Reduction.

HUNG L D (1); IWAMA C (1); BARLI N D (1); SAKAI S (1); TANAKA H (1)
(1) Univ. Tokyo

Joho Shori Gakkai Kenkyu Hokoku, 2003, VOL.2003,NO.119(ARC-155), PAGE.87-92
, FIG.9, REF.11

JOURNAL NUMBER: Z0031BAO ISSN NO: 0919-6072

UNIVERSAL DECIMAL CLASSIFICATION: 681.32.07 621.382.2/.3.049.77

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: **Power consumption** due to leakage increases rapidly as devices scale to smaller geometries. We propose way-variable caches that dynamically adapt the number of active ways according to runtime requirements. By entirely gating the unused ways from the voltage supply, the leakage can be significantly reduced. We then apply an original algorithm utilizing data access locality to make proper resizing decisions. Performance evaluations are done with a superscalar processor model having 16-KB, 4-way set-associative L1 instruction and data **caches**. The results verified that, on average, 1.7 **ways** of the instruction **cache** can be **disabled** with only 1.3% performance degradation in the case of instruction **cache**. The values are 1.5 **ways** and 1.1% in the case of the data **cache**. (author abst.)

DESCRIPTORS: leakage current; CMOS structure; cache memory; performance evaluation; electric **power consumption**; gate(semiconductor); locality; semiconductor chip; pipeline processing; SRAM; energy saving; computer architecture

IDENTIFIERS: instruction cache; data cache; superscalar architecture

BROADER DESCRIPTORS: electric current; MOS structure; device structure; memory(computer); equipment; evaluation; energy consumption; consumption; electrode; property; solid state circuit parts; circuit component; parts; electric apparatus and parts; chip; treatment; RAM; static memory; saving; computer system(architecture); method

CLASSIFICATION CODE(S): JC02040V; NC03162T

18/5/8 (Item 2 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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05569242 JICST ACCESSION NUMBER: 03A0635668 FILE SEGMENT: JICST-E
Design of a Low-Power Cofigurable-Way Cache Applied in Multiprocessor
Systems

CHEN H-C (1); CHIANG J-S (1)

(1) Tamkang Univ., Taipei, Twn

IEICE Trans Inf Syst(Inst Electron Inf Commun Eng), 2003, VOL.E86-D,NO.9,
PAGE.1542-1548, FIG.6, TBL.2, REF.20

JOURNAL NUMBER: L1371AAJ ISSN NO: 0916-8532

UNIVERSAL DECIMAL CLASSIFICATION: 681.32.07

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: In the design of a set-associative cache, maintaining low average access time and reducing the average energy dissipation are important issues. In this paper, we propose a set-associative cache that can provide the flexibility to configure its associativity according to different program behaviors, which means that the proposed **cache** scheme can be configured from n-way set-associative **cache** to direct-mapped **cache**. Besides, the proposed **cache** scheme also can **disable** all **tag**-subarrays and only enable a desired data-subarray when adjacent memory references are within the same **block** as the previous access. By this scheme, the **power consumption** can be **saved** when an n-way set-associative cache configures the cache with lower associativity (less than n) due to only enabling fewer subarrays of the **tag** memory and data memory, and when the **tag** checking is eliminated for the intra- **block** access due to **disabling** all subarrays of the **tag** memory. However, the performance is still maintained to the same as the conventional set-associative **cache** or

the direct-mapped cache. (author abst.)
DESCRIPTORS: cache memory; access time; consumed electric power ;
multiprocessor system; associative memory; reconstitution; element
decomposition; register; block structure; operating system; performance
evaluation; computer simulation
BROADER DESCRIPTORS: memory(computer); equipment; memory characteristic;
characteristic; time; electric power; computer system(hardware); system
; constitution; division and resolution; structure; system program;
computer program; software; evaluation; computer application;
utilization; simulation
CLASSIFICATION CODE(S): JC02040V

18/5/9 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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16050700 PASCAL No.: 03-0199014
Dead-block elimination in cache: A mechanism to reduce I-cache power
consumption in high performance microprocessors
HiPC 2002 : high performance computing : Bangalore, 18-21 December 2002
KABADI Mohan G; KANNAN Natarajan; CHIDAMBARAM Palanidaran; NARAYANAN
Suriya; SUBRAMANIAN M; PARTHASARATHI Ranjani
SARTAJ SAHNI, ed; PRASANNA Viktor K, ed; UDAY SHUKLA, ed
School of Computer Science and Engineering, Anna University, Chennai -
600 025, India
International conference on high performance computing, 9 (Bangalore IND
, 2002-12-18
Journal: Lecture notes in computer science, 2002, 2552 79-88
ISBN: 3-540-00303-7 ISSN: 0302-9743 Availability: INIST-16343;
354000108494050080
No. of Refs.: 18 ref.
Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)
Country of Publication: Germany
Language: English
Both power and performance are important design parameters of the present
day processors. This paper explores an integrated software and circuit
level technique to reduce leakage power in L1 instruction caches of high
performance microprocessors, by eliminating basic blocks from the cache, as
soon as they are dead. The effect of this dead block elimination in cache
on both the power consumption of the I-cache and the performance of the
processor is studied. Identification of basic blocks is done by the
compiler from the control flow graph of the program. This information is
conveyed to the processor, by annotating the first instruction of selected
basic blocks. During execution, the blocks that are not needed further
are traced and invalidated and the lines occupied by them are turned
off. This mechanism yields an average of about 5% to 16% reduction, in
the energy consumed for different sizes of I- cache, for a set of the SPEC
CPU 2000 benchmarks (16), without any performance degradation.

English Descriptors: Graph flow; High performance; Microprocessor; Control
program; Integrated circuit; Compiler; Data flow; AND circuit; Energy
consumption

French Descriptors: Flot graphe; Haute performance; Microprocesseur;
Programme commande; Circuit integre; Compilateur; Flot donnee; Circuit ET
; Consommation energie; Dead-block elimination

Classification Codes: 001D02B10; 001D03F06B
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18/5/10 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
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15194794 PASCAL No.: 01-0360017

Cache-line decay: A mechanism to reduce cache leakage power

PACS 2000 : power-aware computer systems : Cambridge MA, 12 November 2000, revised papers

KAXIRAS Stefanos; ZHIGANG HU; NARLIKAR Girija; MCLELLAN Rae
FALSAFI B, ed; VIJAYKUMAR TN, ed

Bell Laboratories, Lucent Technologies , United States; Princeton University, United States

Power-aware computer systems. International workshop, 1 (Cambridge MA USA) 2000-11-12

Journal: Lecture notes in computer science, 2001, 2008 82-96

ISBN: 3-540-42329-X ISSN: 0302-9743 Availability: INIST-16343;
354000092488330070

No. of Refs.: 15 ref.

Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)

Country of Publication: Germany

Language: English

Reducing the supply voltage to reduce dynamic power consumption in CMOS devices, inadvertently will lead to an exponential increase in leakage power dissipation. In this work we explore an architectural idea to reduce leakage power in data caches. Previous work has shown that cache frames are "dead" for a significant fraction of time (14). We are exploiting this observation to turn off cache lines that are not likely to be accessed any more. Our method is simple: if a cache - line is not accessed within a fixed interval (called decay interval) we turn off its supply voltage using a gated V SUB d SUB d technique introduced previously (12). We study the effect of cache - line decay on both power consumption and performance. We find that it is possible with cache-line decay to build larger caches that dissipate less leakage power than smaller caches while yielding equal or better performance (fewer misses). In addition, because our method can dynamically trade performance for leakage power it can be adjusted according to the requirements of the application and/or the environment.

English Descriptors: Circuit design; Cache memory; Power supply; Voltage; Leakage current; Complementary MOS technology; Energy consumption; Energy dissipation; Off line

French Descriptors: Conception circuit; Antememoire; Alimentation electrique; Tension electrique; Courant fuite; Technologie MOS complementaire; Consommation energie; Dissipation energie; Hors ligne

Classification Codes: 001D03F06B

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18/5/11 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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12015797 Genuine Article#: 720TL Number of References: 20

Title: Design of a low-power configurable-way cache applied in multiprocessor systems

Author(s): Chen HC (REPRINT) ; Chiang JS

Corporate Source: Tamkang Univ, Dept Elect Engn, 151 Ying Chuan Rd/Taipei 25137//Taiwan/ (REPRINT); Tamkang Univ, Dept Elect Engn, Taipei 25137//Taiwan/

Journal: IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS, 2003, VE86D, N9 (SEP), P1542-1548

ISSN: 0916-8532 Publication date: 20030900

Publisher: IEICE-INST ELECTRONICS INFORMATION COMMUNICATIONS ENG, KIKAI-SHINKO-KAIKAN BLDG MINATO-KU SHIBAKOEN 3 CHOME, TOKYO, 105, JAPAN

Language: English Document Type: ARTICLE

Geographic Location: Taiwan

Subfile: AHSearch

Journal Subject Category: COMPUTER SCIENCE, INFORMATION SYSTEMS; COMPUTER SCIENCE, SOFTWARE ENGINEERING

Abstract: In the design of a set-associative cache, maintaining low average

access time and reducing the average energy dissipation are important issues. In this paper, we propose a set-associative cache that can provide the flexibility to configure its associativity according to different program behaviors, which means that the proposed cache scheme can be configured from n-way set-associative cache to direct-mapped cache. Besides, the proposed cache scheme also can disable all tag-subarrays and only enable a desired data-subarray when adjacent memory references are within the same block as the previous access. By this scheme, the power consumption can be saved when an n-way set-associative cache configures the cache with lower associativity (less than n) due to only enabling fewer subarrays of the tag memory and data memory, and when the tag checking is eliminated for the intra-block access due to disabling all subarrays of the tag memory. However, the performance is still maintained to the same as the conventional set-associative cache or the direct-mapped cache.

Descriptors--Author Keywords: configurable-way ; intra-block access ; average energy dissipation ; previous block register (PBR) ; multiprocessor systems

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18/5/12 (Item 2 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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11587662 Genuine Article#: BW58C Number of References: 18

Title: Dead-block elimination in cache: A mechanism to reduce I-cache power consumption in high performance microprocessors

Author(s): Kabadi MG (REPRINT) ; Kannan N; Chidambaram P; Narayanan S; Subramanian M; Parthasarathi R

Corporate Source: Anna Univ,Sch Engn & Comp Sci,Madras 600025/Tamil Nadu/India/ (REPRINT); Anna Univ,Sch Engn & Comp Sci,Madras 600025/Tamil Nadu/India/

, 2002, V2552, P79-88

ISSN: 0302-9743 Publication date: 20020000

Publisher: SPRINGER-VERLAG BERLIN, HEIDELBERGER PLATZ 3, D-14197 BERLIN, GERMANYHIGH PERFORMANCE COMPUTING - HIPC 2002, PROCEEDINGS

Series: LECTURE NOTES IN COMPUTER SCIENCE

Language: English Document Type: ARTICLE

Geographic Location: India

Journal Subject Category: COMPUTER SCIENCE, THEORY & METHODS

Abstract: Both power and performance are important design parameters of the present day processors. This paper explores an integrated software and circuit level technique to reduce leakage power in L1 instruction caches of high performance microprocessors, by eliminating basic blocks from the cache, as soon as they are dead. The effect of this dead block elimination in cache on both the power consumption of the I-cache

and the performance of the processor is studied. Identification of basic blocks is done by the compiler from the control flow graph of the program. This information is conveyed to the processor, by annotating the first instruction of selected basic blocks. During execution, the blocks that are not needed further are traced and invalidated and the lines occupied by them are turned off. This mechanism yields an average of about 5% to 16% reduction, in the energy consumed for different sizes of I-cache, for a set of the SPEC CPU 2000 benchmarks [16], without any performance degradation.

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18/5/13 (Item 1 from file: 95)

DIALOG(R)File 95:TEME-Technology & Management
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01727677 20030107546

Dead-block elimination in cache: a mechanism to reduce I-cache power consumption in high performance microprocessors

(Dead-block-Eliminierung im Cache: ein Mechanismus zur Reduzierung der I-Cache-Stromaufnahme in Hochleistungs-Mikroprozessoren)

Kabadi, MG; Kannan, N; Chidambaram, P; Narayanan, S; Subramanian, M; Parthasarathi, R

Anna Univ., Chennai (Madras), IND

HIPC 2002, High Performance Computing, 9th Internat. Conf., Proc., Bangalore, IND, Dec 18-21, 2002Lecture Notes in Computer Science, v2552, n11, pp79-88, 2002

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Record type: Abstract

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ABSTRACT:

Both power and performance are important design parameters of the present day processors. This paper explores an integrated software and circuit level technique to reduce leakage power in L1 instruction caches of high performance microprocessors, by eliminating basic blocks from the cache, as soon as they are dead. The effect of this dead blocks elimination in cache on both the power consumption of the I-cache and the performance of the processor is studied. Identification of basic blocks is done by the compiler from the control flow graph of the program. This information is conveyed to the processor, by annotating the first instruction of selected basic blocks. During execution, the blocks that are not needed further are traced and invalidated and the lines occupied by them are turned off. This mechanism yields an average of about 5 % to 16 % reduction, in the energy consumed for different sizes of I-cache, for a set of the SPEC CPU 2000 benchmarks, without any performance degradation.

DESCRIPTORS: CACHE MEMORIES; INPUT--POWER; MICROPROCESSORS; HIGH PERFORMANCE; COMPILERS; IMPROVEMENT; FLOW CHARTS; TIMING CHART; PROGRAM

INSTRUCTION; BENCHMARKING
IDENTIFIERS: SPEC 2000--(BENCHMARK); PUNKTMENGENDARSTELLUNG;
L1-Instruktions-Cache; Dead-Code-Eliminierung; Compiler

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Drowsy caches: simple techniques for reducing leakage power

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ARM Ltd., Cambridge, GB

Proceedings 29th Annual International Symposium on Computer Architecture,
25-29 May 2002, Anchorage, AK, USA2002

Document type: Conference paper Language: English

Record type: Abstract

ISBN: 0-7695-1605-X

ABSTRACT:

On-chip caches represent a sizable fraction of the total **power consumption** of microprocessors. Although large caches can significantly improve performance, they have the potential to increase **power consumption**. As feature sizes shrink the dominant component of this power loss will be leakage. However, during a fixed period of time the activity in a cache is only centered on a small subset of the lines. This behavior can be exploited to cut the leakage power of large caches by putting the cold cache lines into a state **preserving**, low- **power** drowsy mode. Moving lines into and out of drowsy state incurs a slight performance loss. In this paper we investigate policies and circuit techniques for implementing drowsy caches. We show that with simple architectural techniques, about 80%-90% of the cache lines can be maintained in a drowsy state without affecting performance by more than 1%. According to our projections, in a 0.07 um CMOS process, drowsy caches will be able to reduce the total energy (static and dynamic) consumed in the **caches** by 50%-75%. We also argue that the use of drowsy **caches** can simplify the design and control of low-leakage **caches**, and avoid the need to completely **turn off** selected **cache lines** and lose their state.

DESCRIPTORS: CACHE MEMORIES; CMOS CIRCUITS; MEMORY ELEMENTS; MEMORY ARCHITECTURE; INPUT--POWER

IDENTIFIERS: GESAMTENERGIE; Cache-Speicher; Komplementaere Mos-Schaltung

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PowerPC 603, a microprocessor for portable computers

(PowerPC 603, ein Mikroprozessor fuer tragbare Rechner)

Gary, S; Ippolito, P; Gerosa, G; Dietz, C; Eno, J; Sanchez, H

IEEE Design and Test of Computers, v11, n4, pp14-23, 1994

Document type: journal article Language: English

Record type: Abstract

ISSN: 0740-7475

ABSTRACT:

The PowerPC 603 incorporates a variety of features to reduce power dissipation: dynamic idle-time **shutdown** of separate execution **units**, low-power **cache** design, and power considerations for standard cells, data-path **elements**, and clocking. System-level features include three software-programmable static power management modes and a hardware-programmable phase-lock loop. Operating at 80 MHz, the 603 typically dissipates 2.2 W, while achieving an estimated 75 Specint92 and 85 Specfp92.

DESCRIPTORS: MICROPROCESSORS; PORTABLE COMPUTERS; DISSIPATION **POWER** ;

MEMORIES; ENERGY CONSUMPTION;
AMPLIFIERS; COMPUTER POWER SUPPLIES; DYNAMIC IDLE TIME SHUTDOWN; LOW POWER
CIRCUIT DESIGN; SOFTWARE PROGRAMMABLE; STATIC POWER MANAGEMENT MODES;
HARDWARE PROGRAMMABLE; PHASE LOCK LOOP; Mikroprozessor; tragbarer Rechner

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**Analysis of the Intel 386 and i486 microprocessors for the space station
Freedom data management system**

(Analyse der Mikroprozessoren Intel 386 und i486 fuer das
Datenverwaltungssystem der Raumstation Freedom)

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NASA Ames Res. Center, Moffett Field, USA

AIAA Computing in Aerospace 8, Volume 2, Baltimore, USA, October 21-24,
1991/1991

Document type: Conference paper Language: English

Record type: Abstract

ABSTRACT:

This report analyzes the feasibility of upgrading the Intel 386 microprocessor, which has been proposed as the baseline processor for the Space Station Freedom (SSF) Data Management System (DMS), to the more advanced i486 microprocessor. The items compared between the two processors include the instruction set architecture, **power consumption**, the MIL-STD-883C Class S (space) qualification schedule, and performance. The advantages of the i486 over the 386 are lower **power consumption** and higher floating-point performance in speed. The i486 on-chip **cache**, however, has neither parity check nor error detection and correction circuitry. The i486 with on-chip **cache disabled**, however, has lower integer performance in speed than the 386 without **cache**, which is the current DMS design choice. The benchmark performance of a 386-based prototype Flight Equivalent **Unit** (FEU), which is the closest configuration to the DMS design as of April 1991, is only about 50 % of a PS/2 Model 70 with cache, which is generally considered as a 4 MIPS (million instructions per second) computer. Adding cache to the 386/387 DX memory hierarchy appears to be the most beneficial way to enhance computation-intensive performance for the current DMS design at this time.